

COMPAL CONFIDENTIAL

MODEL NAME : CDP70
PCB NO : LA-E141P
BOM P/N :
GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 14 UMA

Kabylake H


2016-07-01

REV : 0.2 (X01)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESD Component
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component

MB PCB	
Part Number	Description
DAB0001R000	PCB 1SC LA-E141P REV0 MB UMA 1

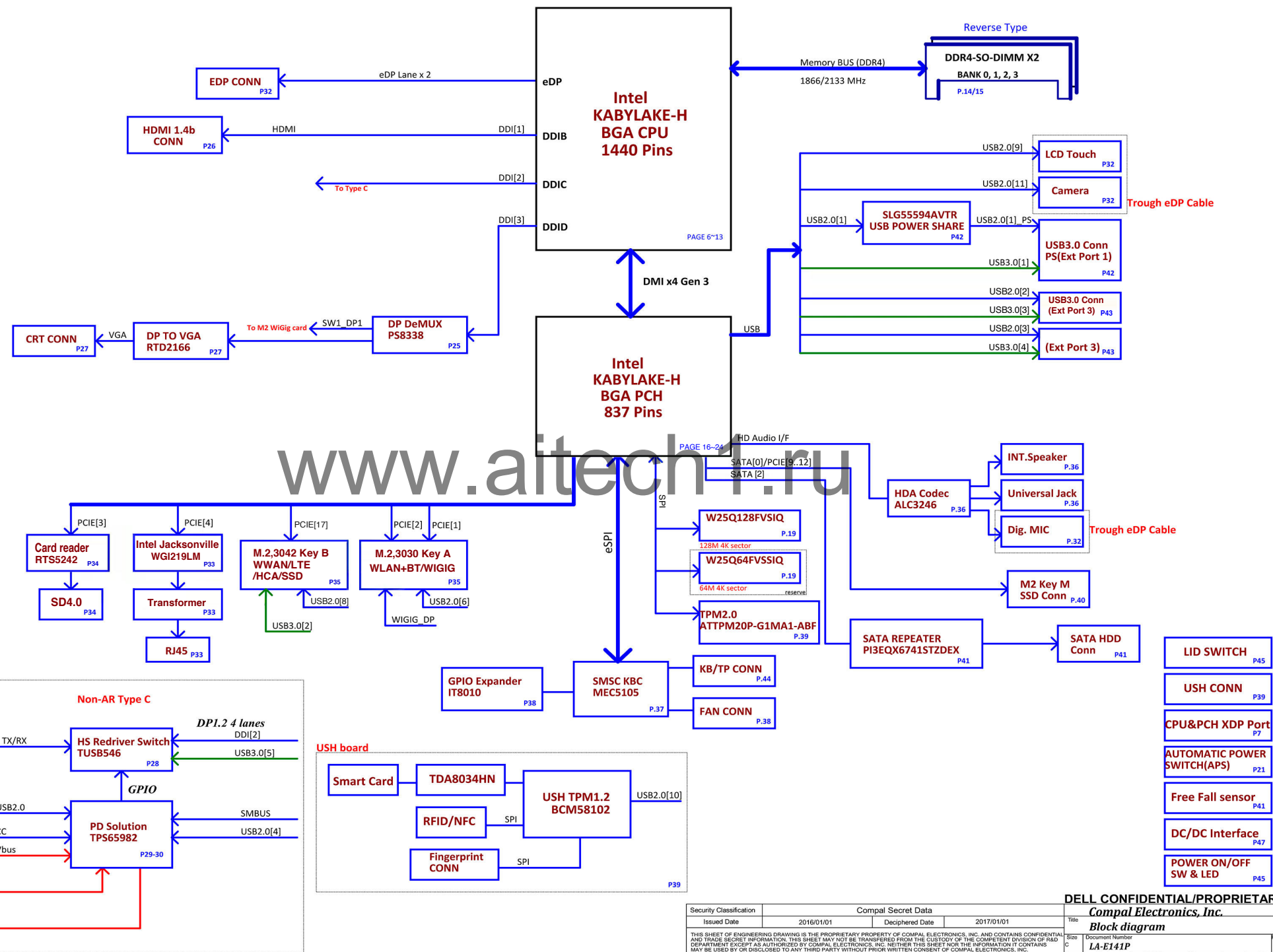
Layout Dell logo

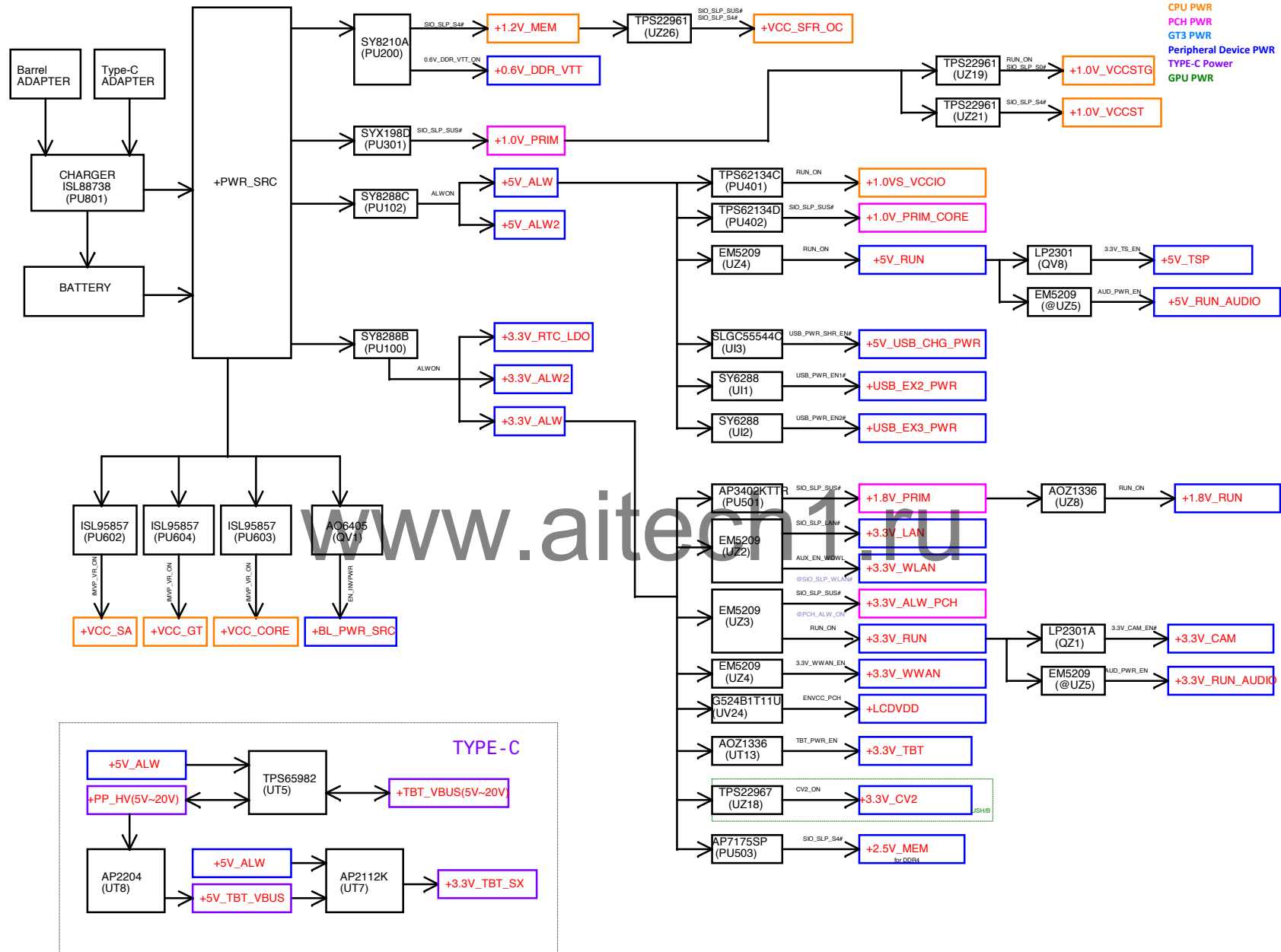


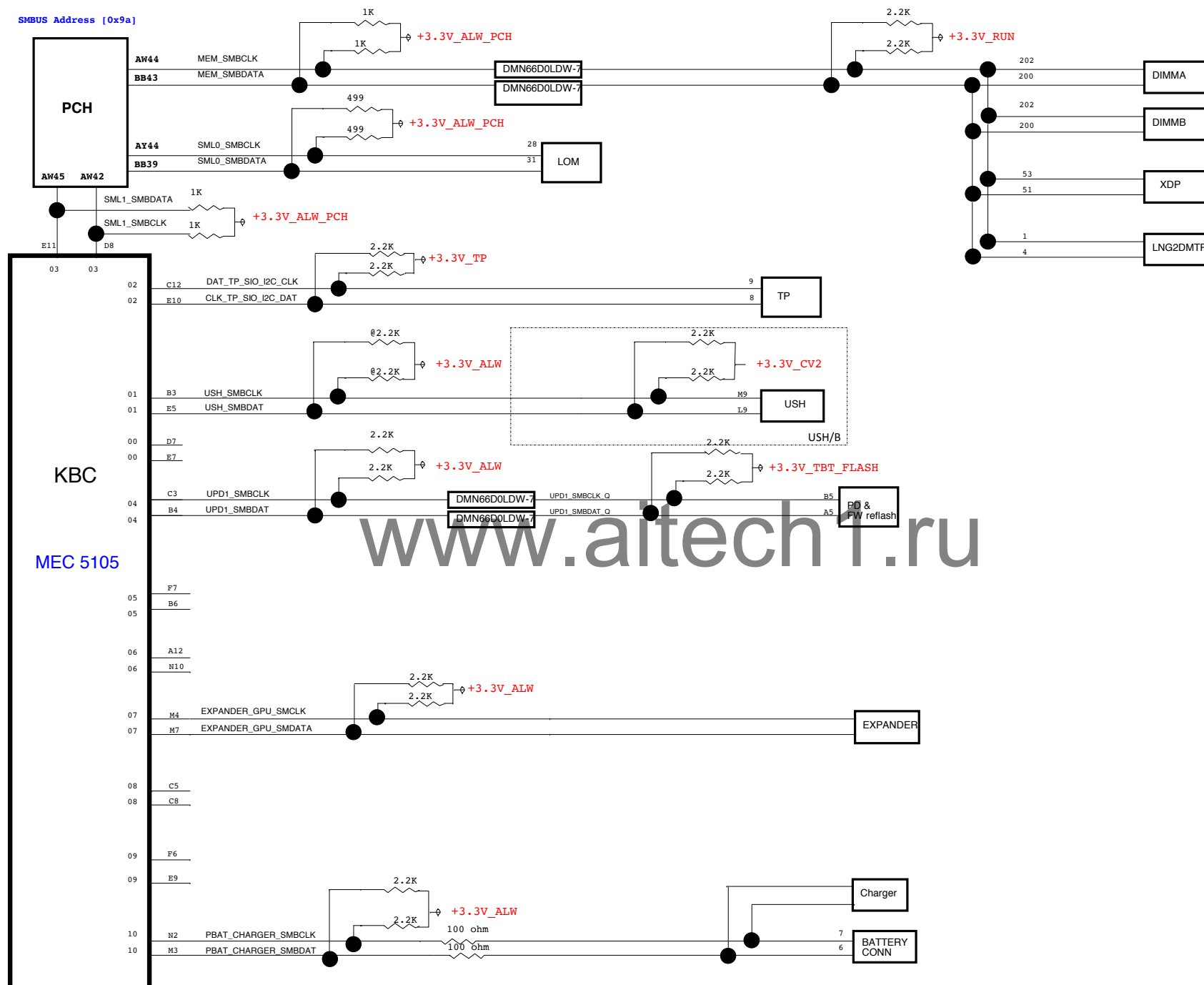
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Title		Compal Electronics, Inc.		Cover Sheet	
Size A		Document Number		Rev 0.2	
Date: Friday, July 01, 2016		Sheet 1 of 61		LA-E141P	
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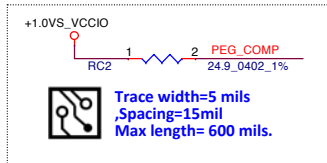
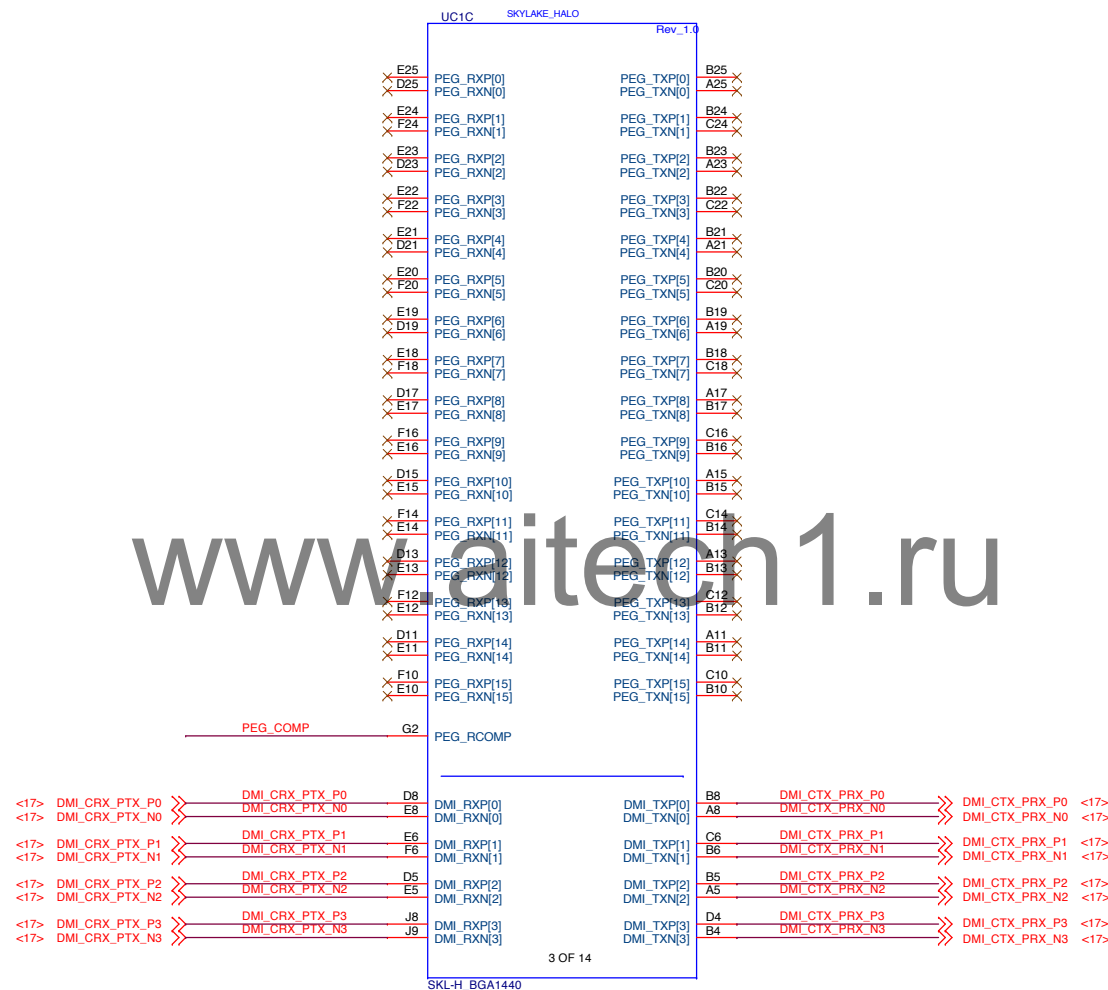
Breckenridge 14 UMA non-TBT Block Diagram



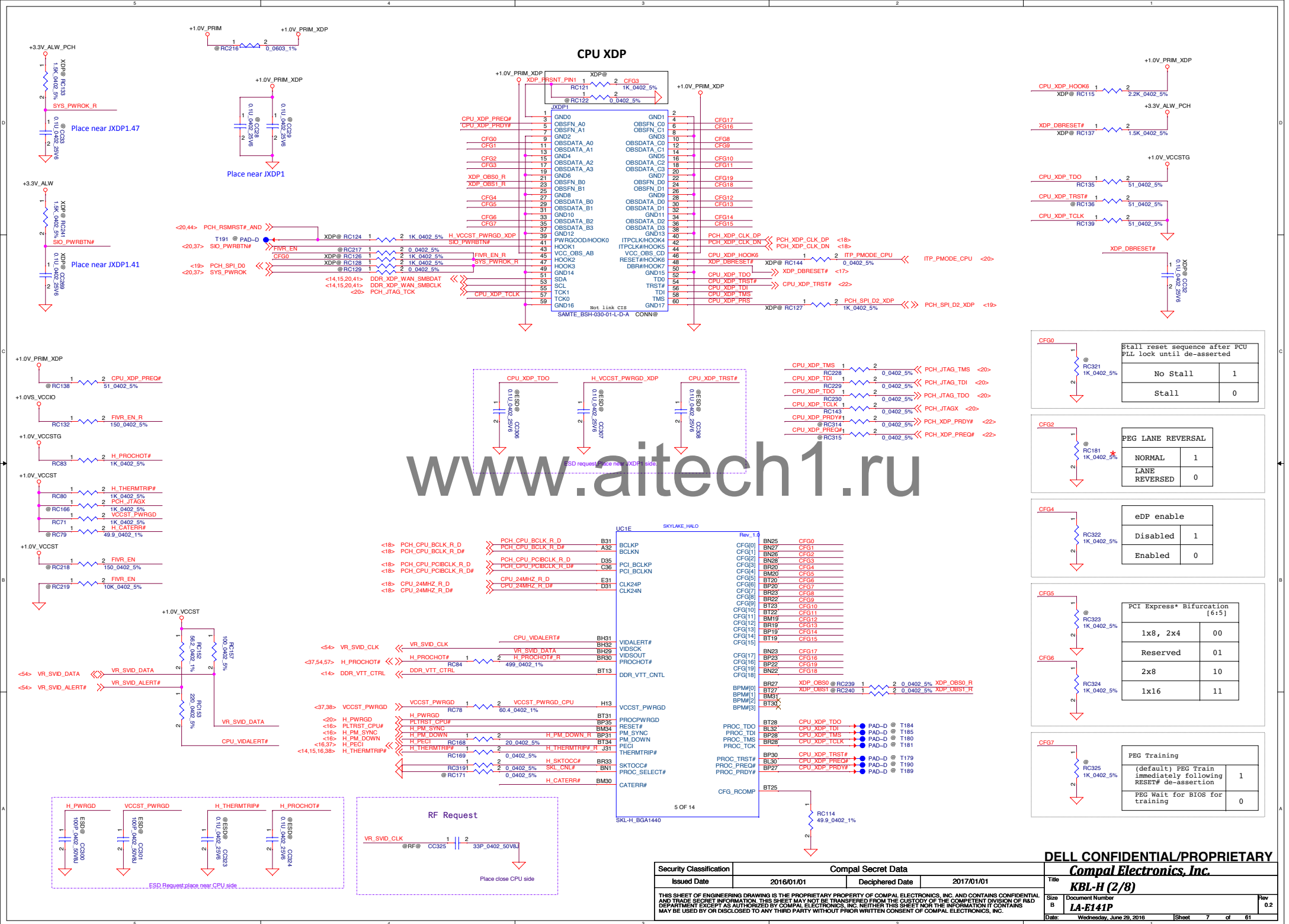


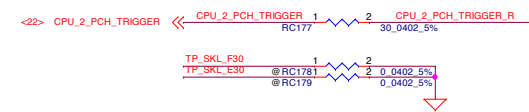
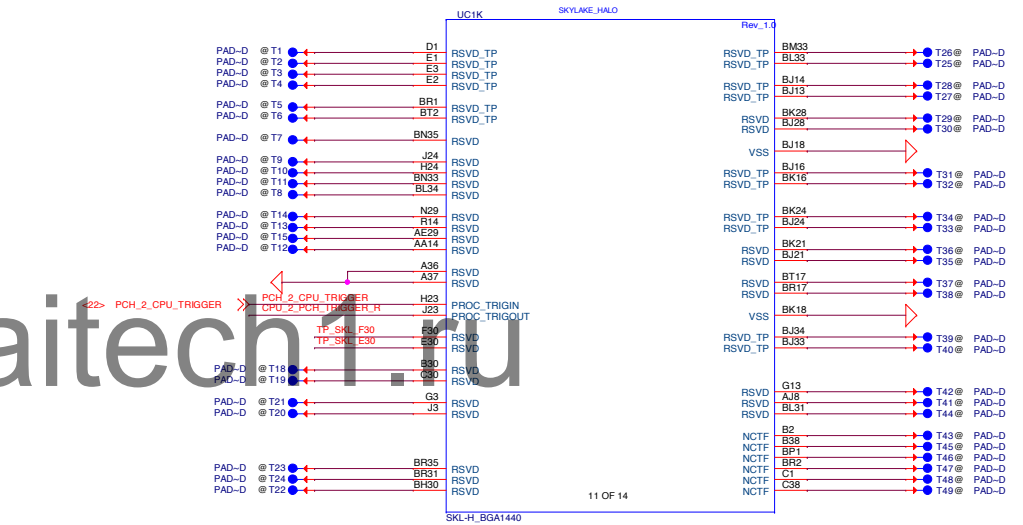
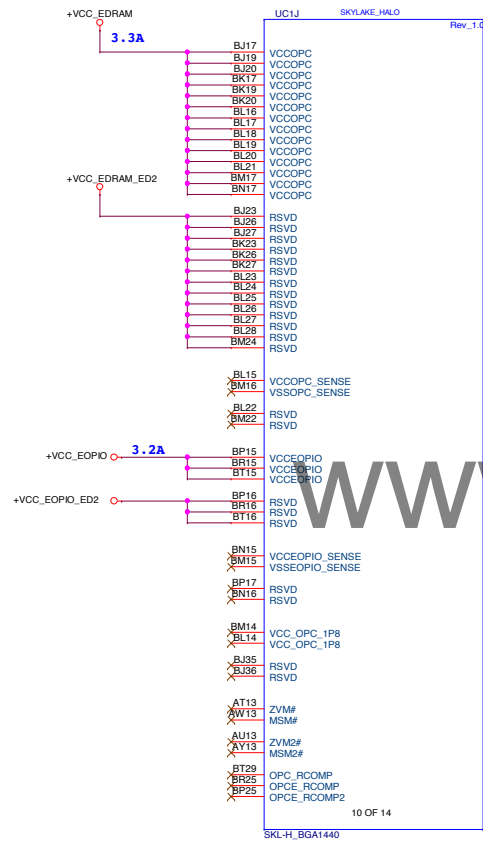


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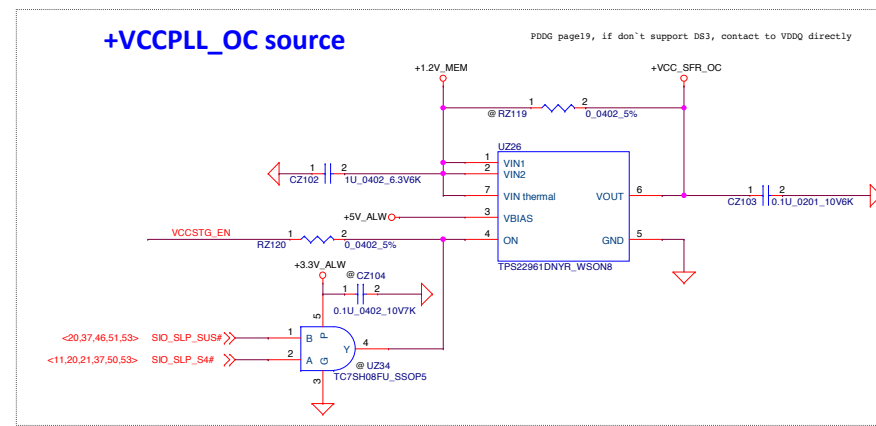
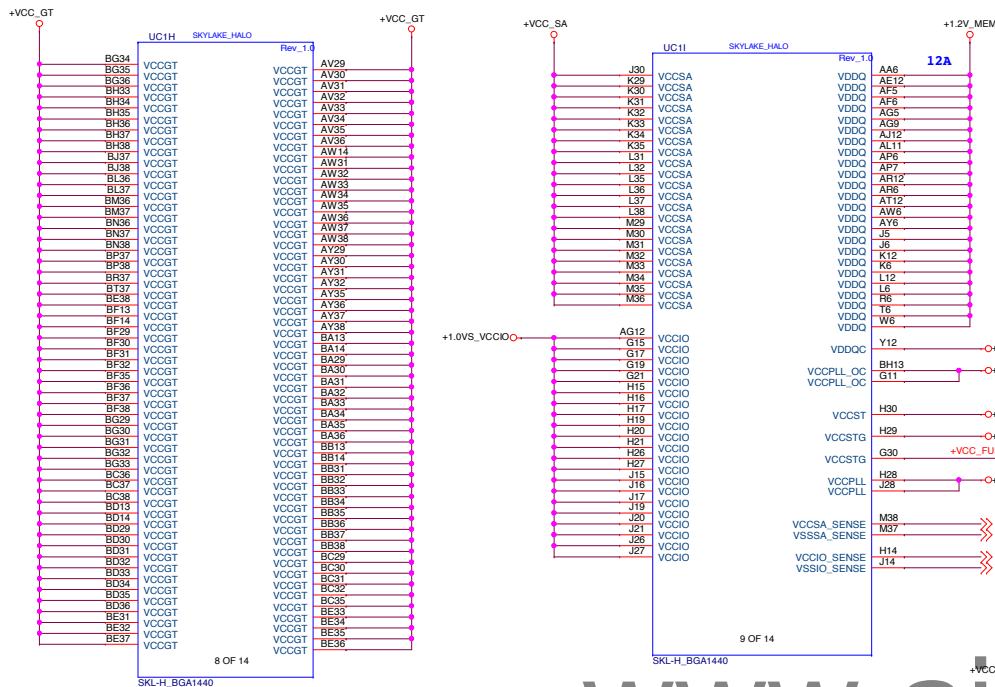


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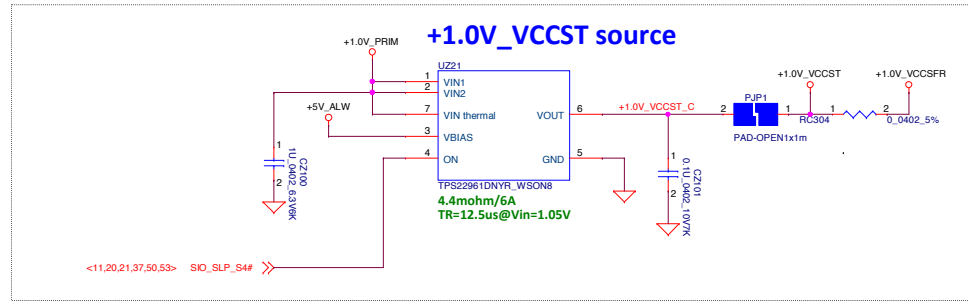
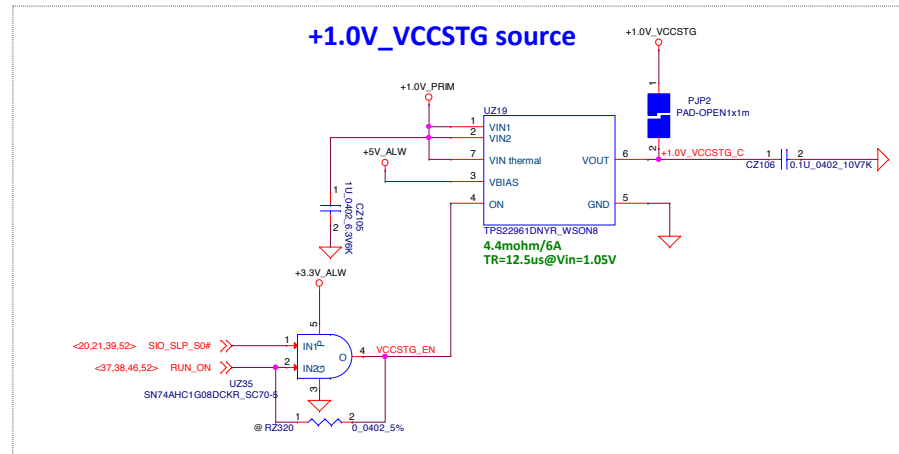




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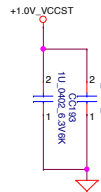
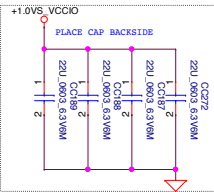
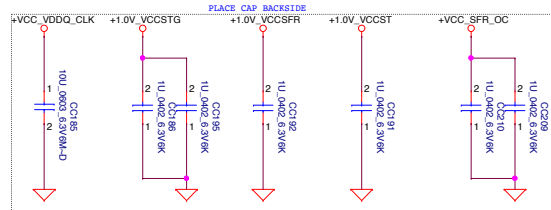


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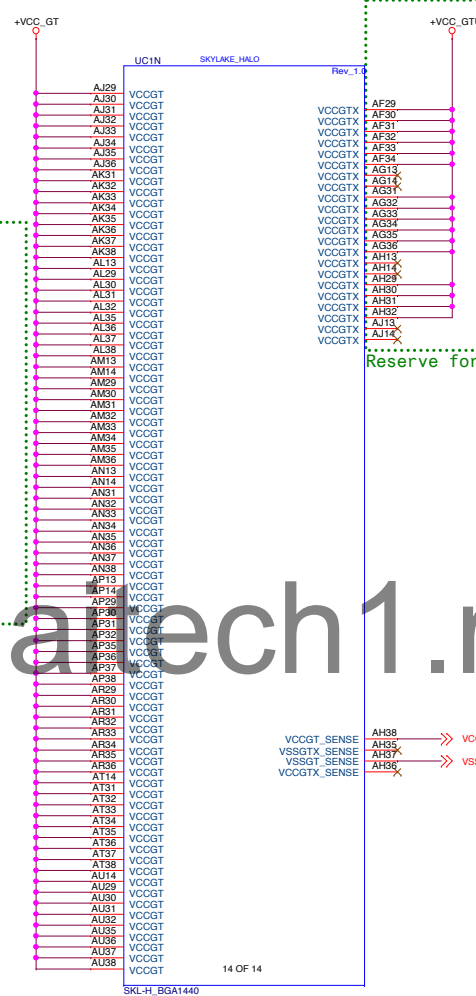
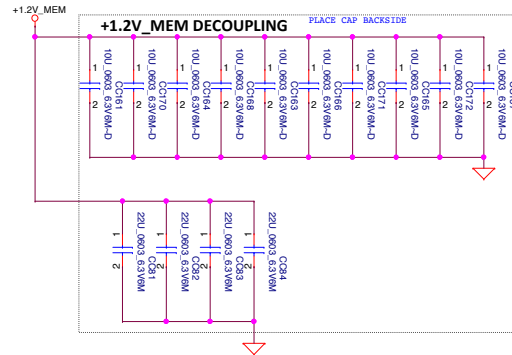


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For SKL-H 4+2
Remove VCCOPC/VCCEPIO/
VCCOPC_1P8 Cap



Remove to Power (+VCC_SA cap)



VCCGT_SENSE AH38 >>> VCC_GT_SENSE <54>
VSSGT_SENSE AH35 >>> VSS_GT_SENSE <54>
VCCGT_SENSE AH37 >>> VSS_GT_SENSE <54>
VCCGT_SENSE AH36 >>> VSS_GT_SENSE <54>



VSS_SENSE 1 2 49.9_0402_1%
VCC_SENSE 1 2 49.9_0402_1%

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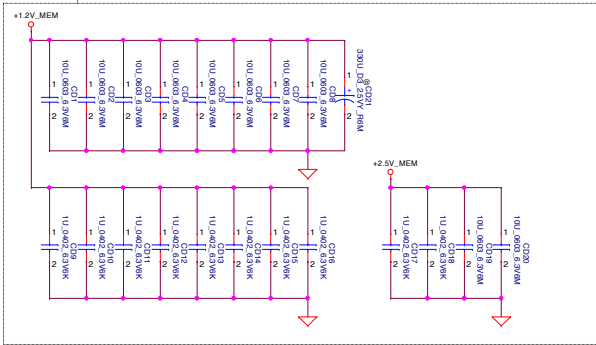
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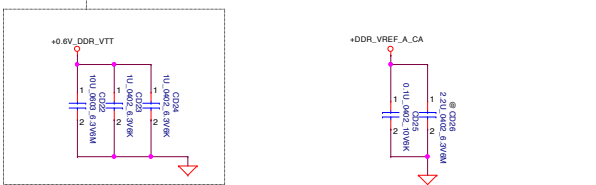
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 DQR_A_DQ[15:15]
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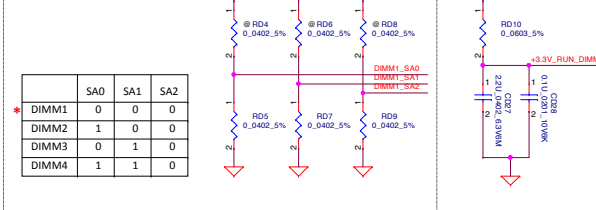
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Layout Note:
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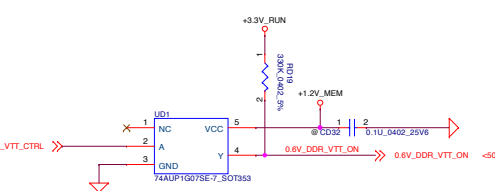
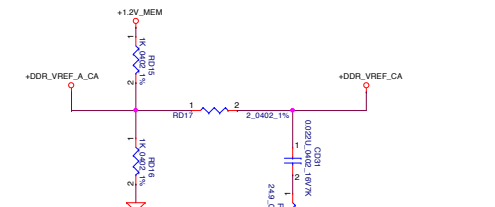
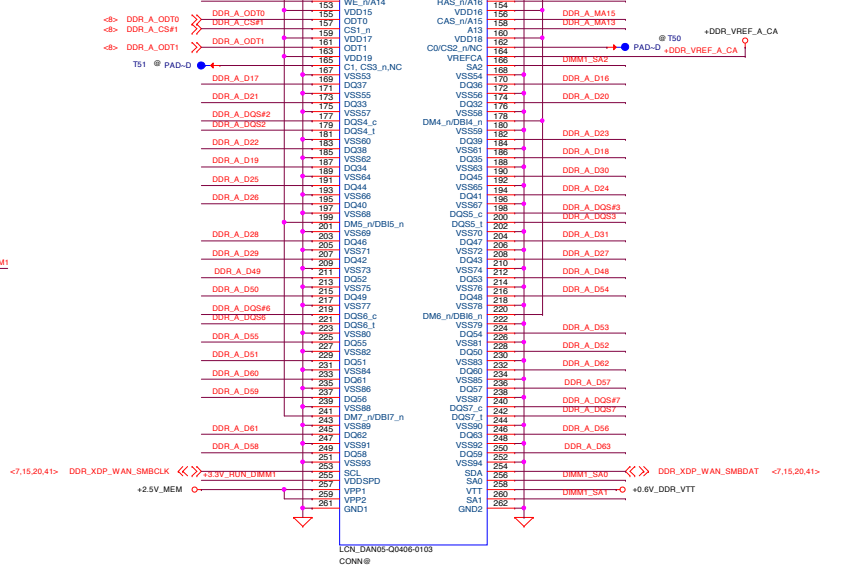


DIMM Select



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Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
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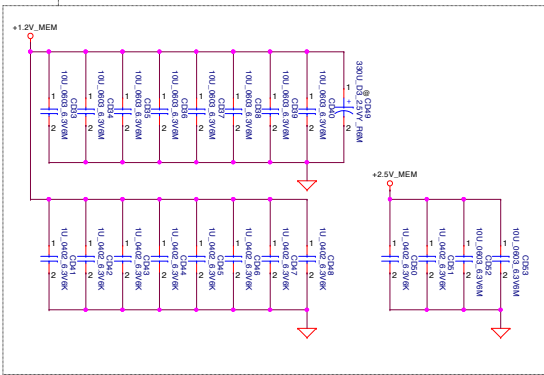
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DDR4-SODIMM SLOT1

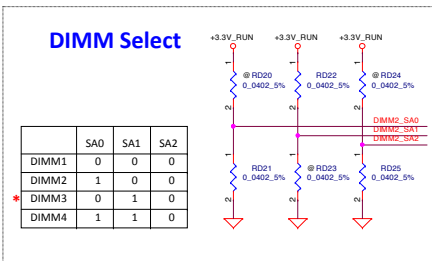
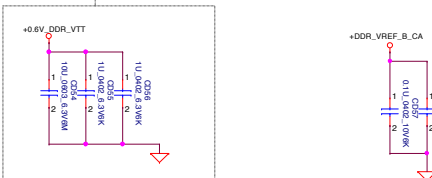
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DDR_B_DQS#0..7
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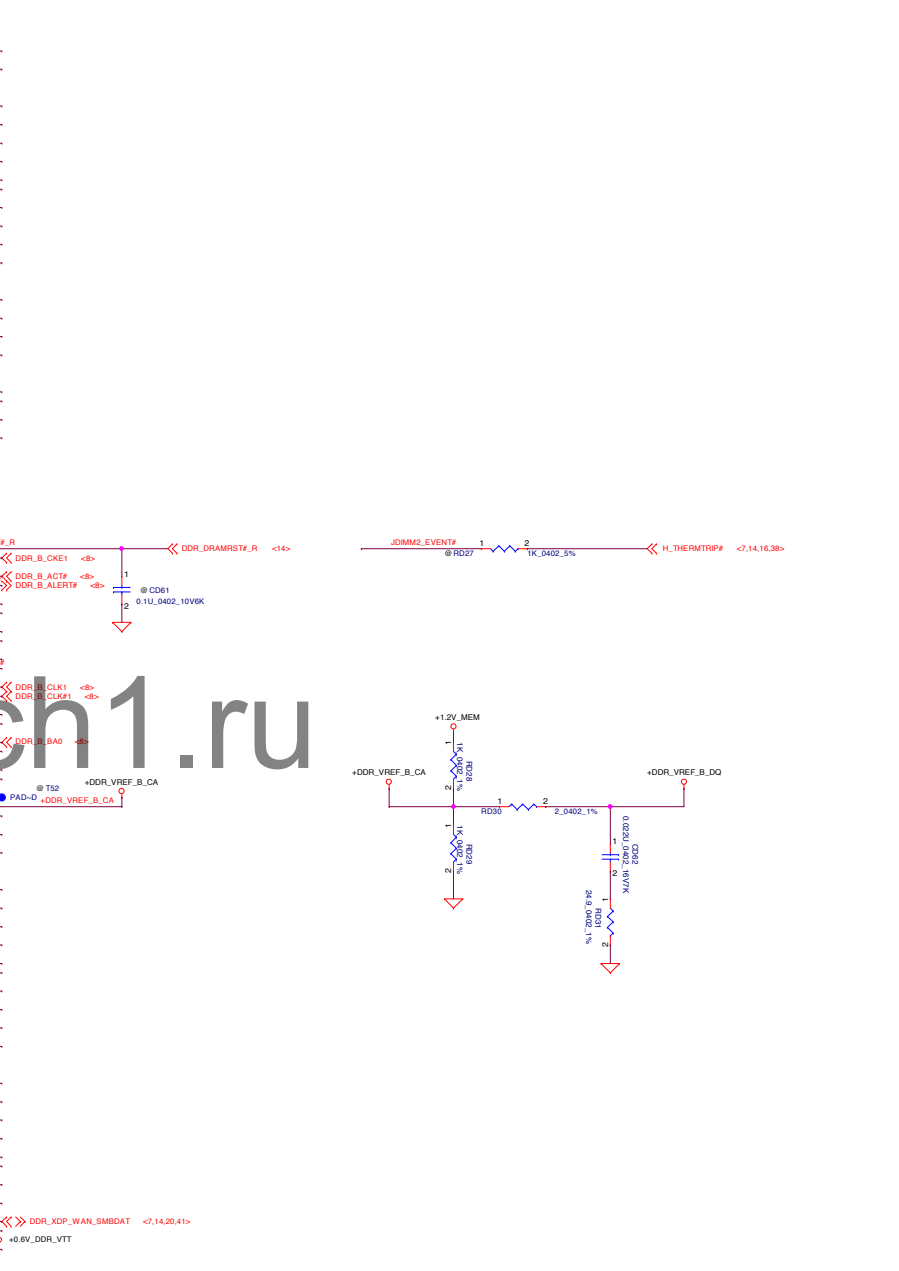
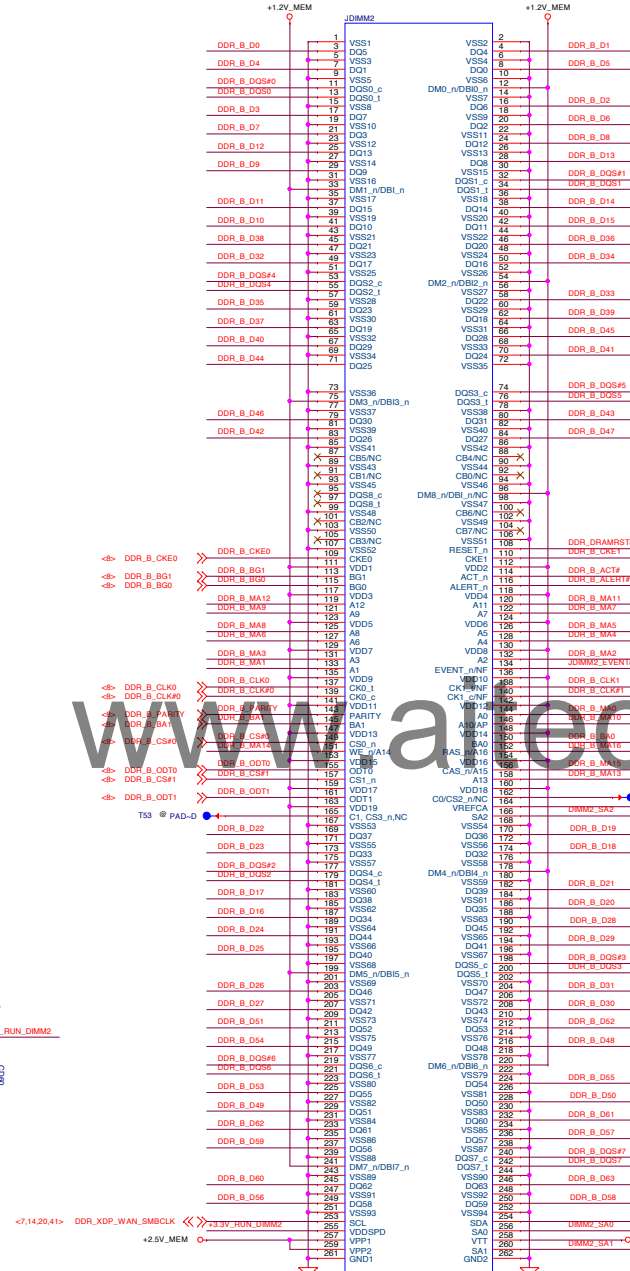
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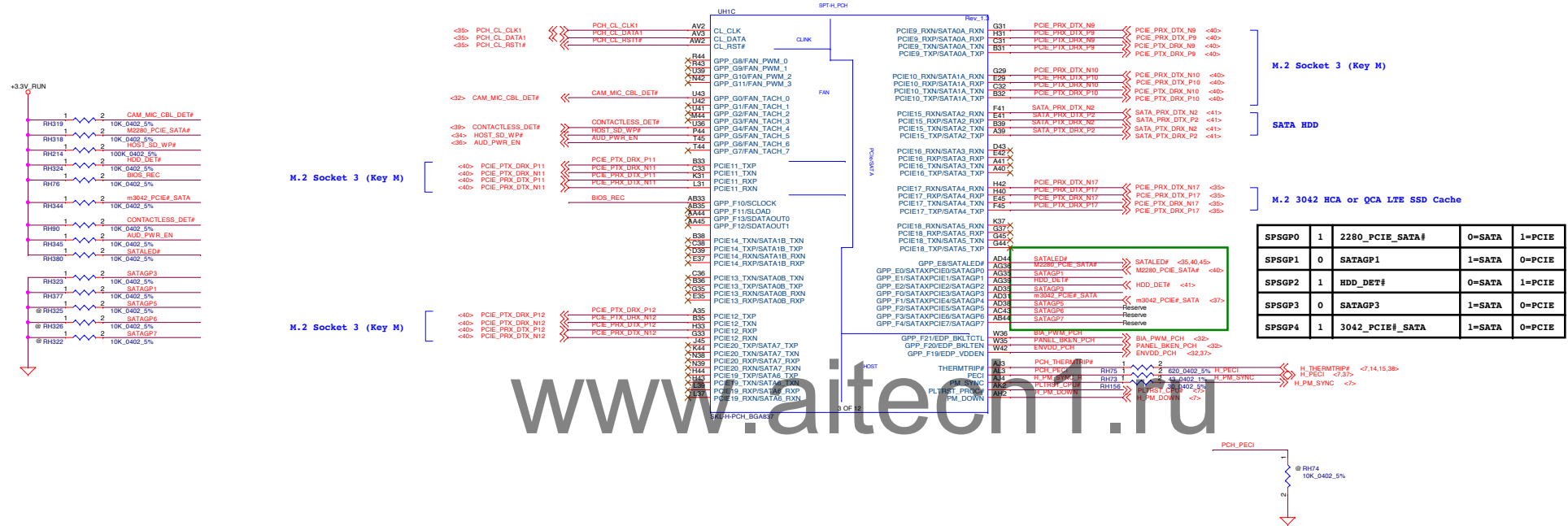


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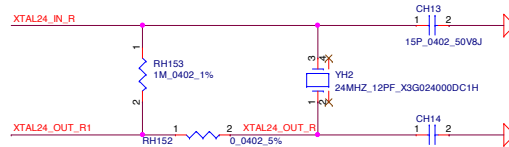
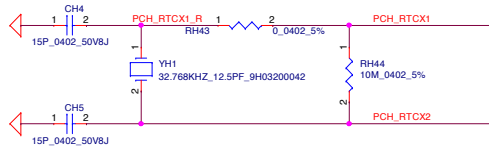
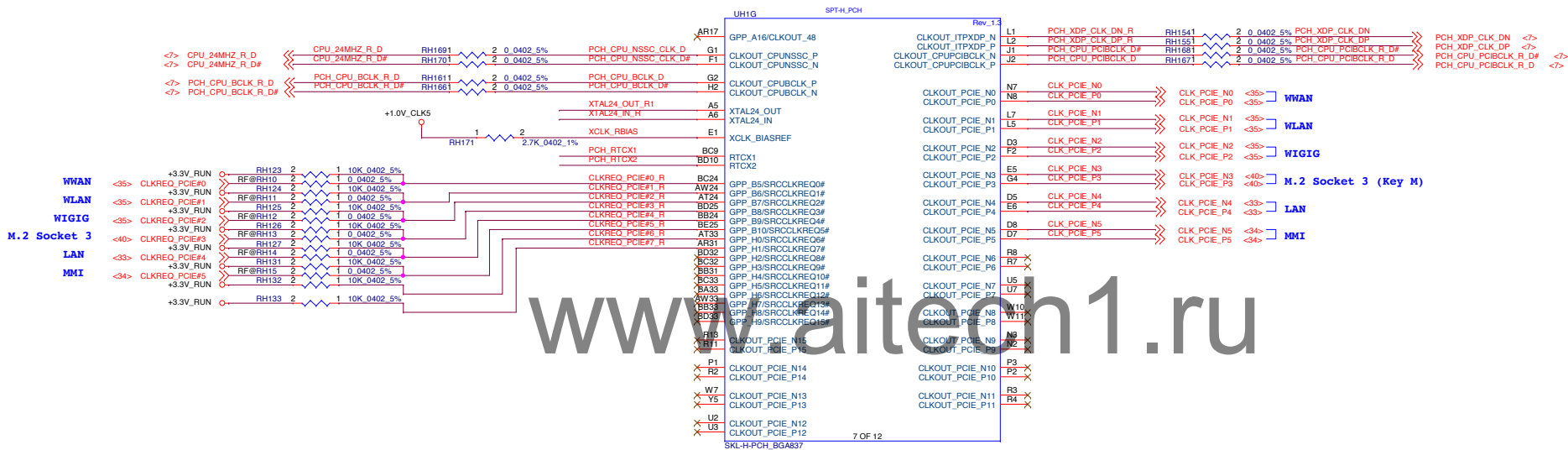
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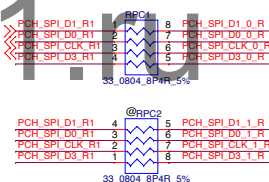
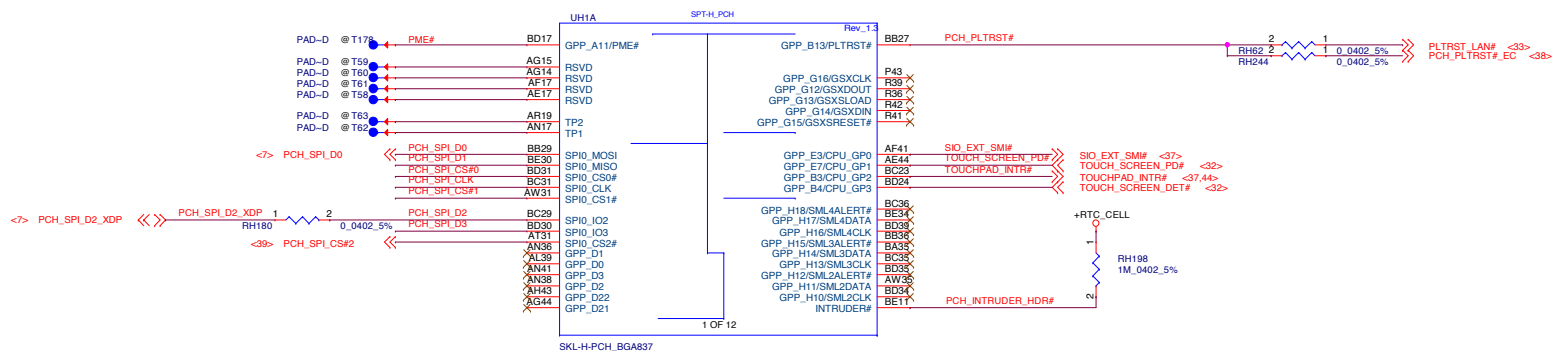
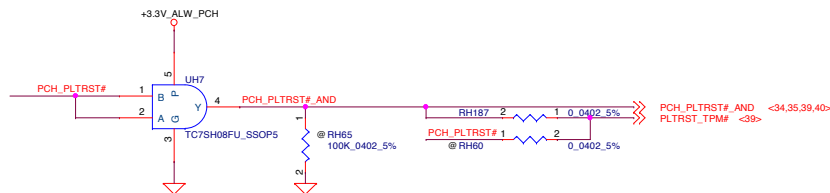
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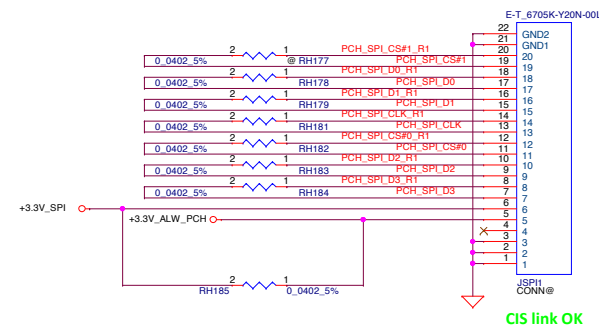
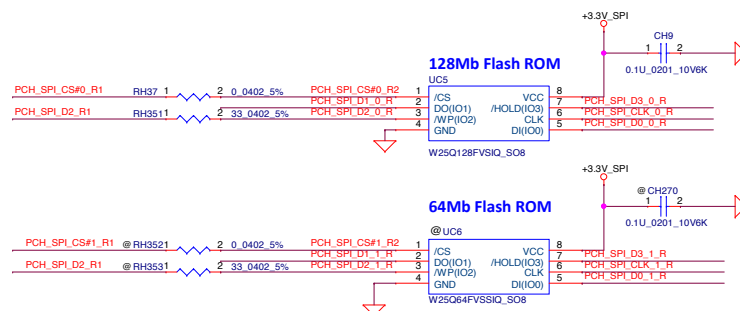


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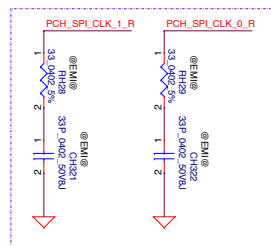
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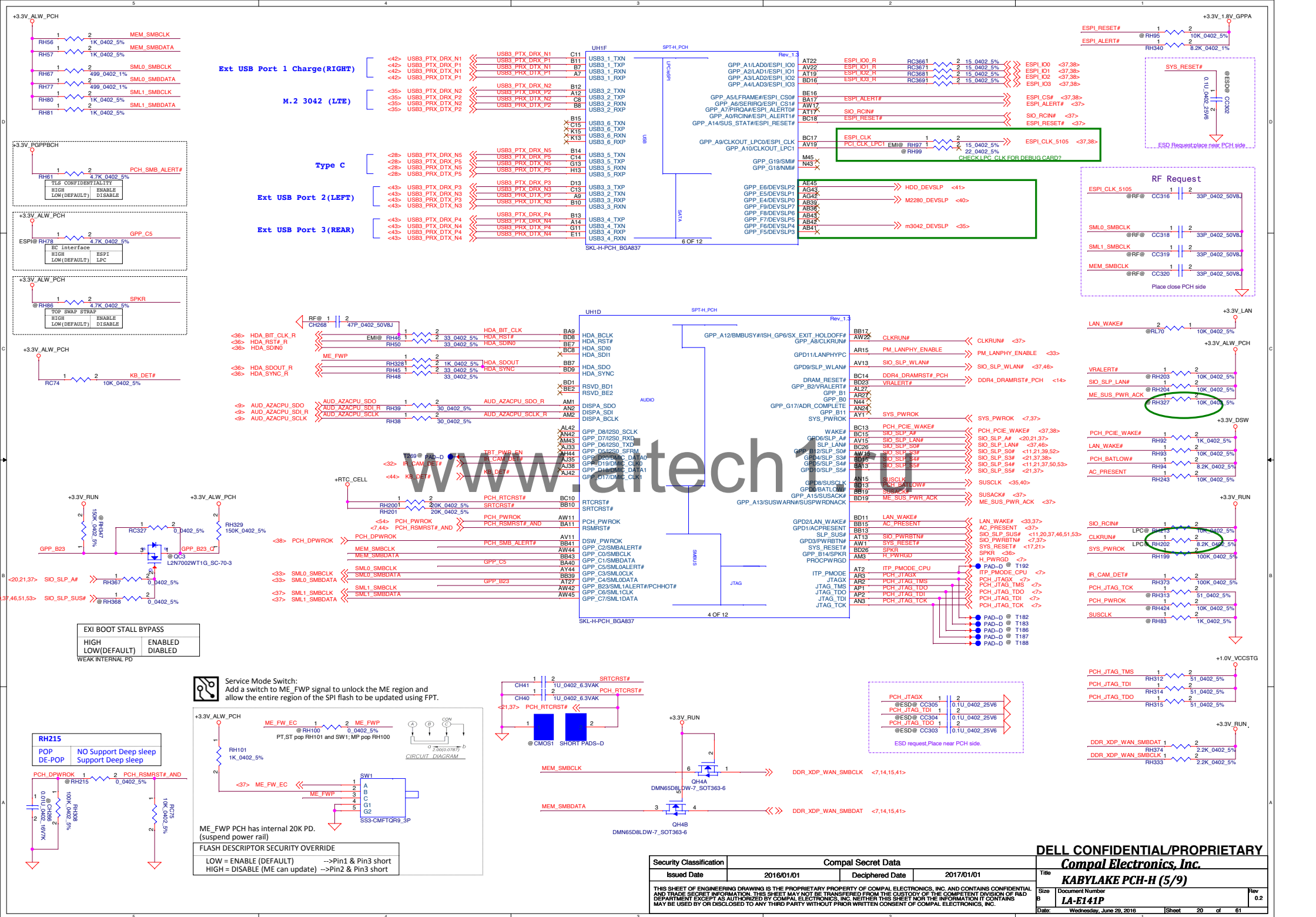
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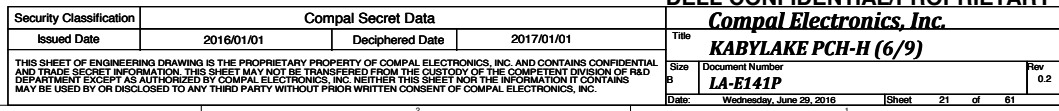


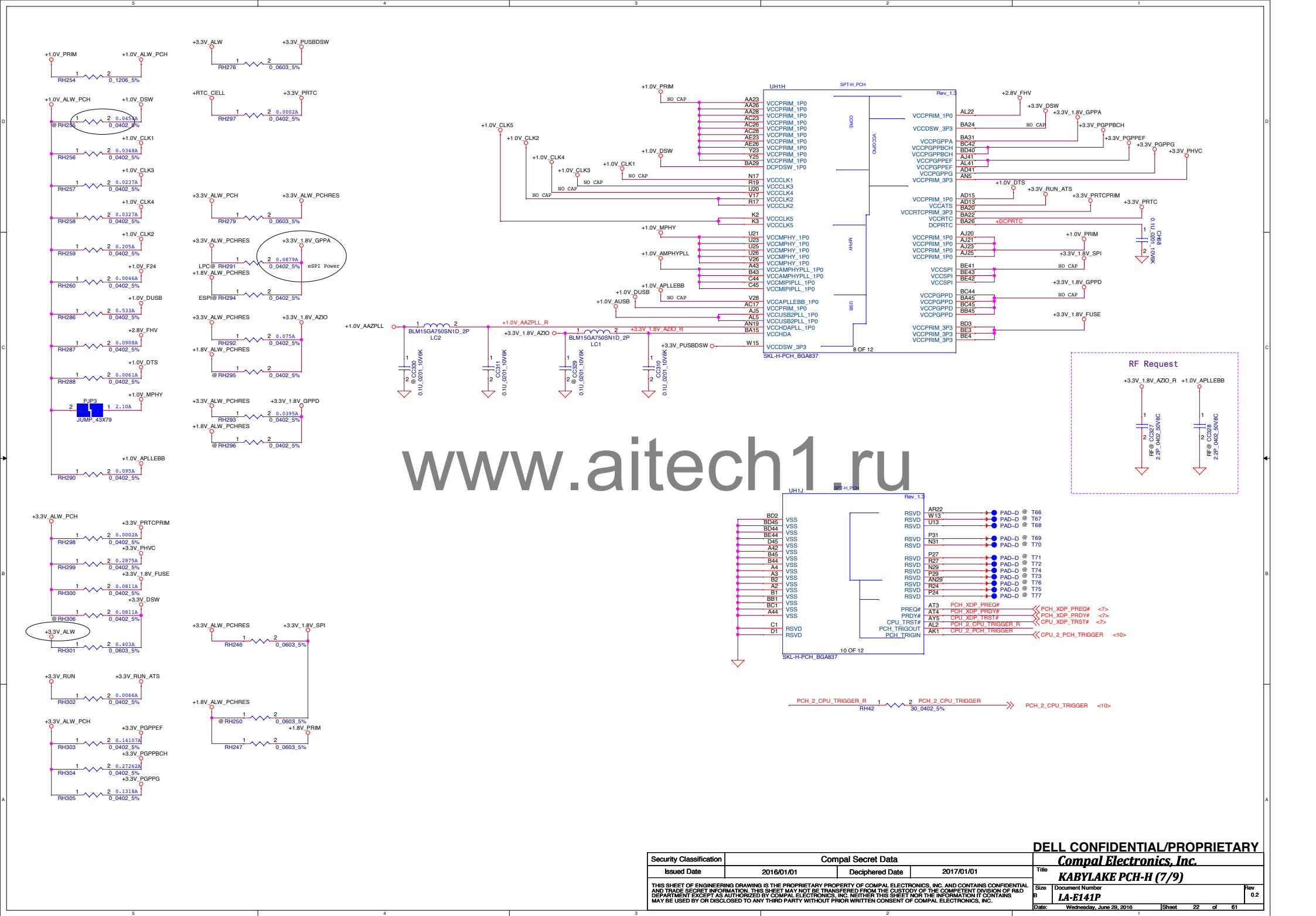
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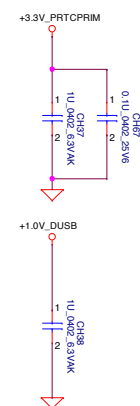
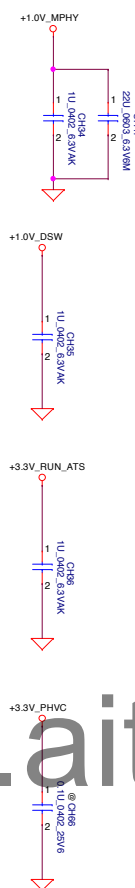
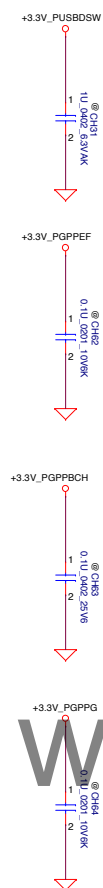
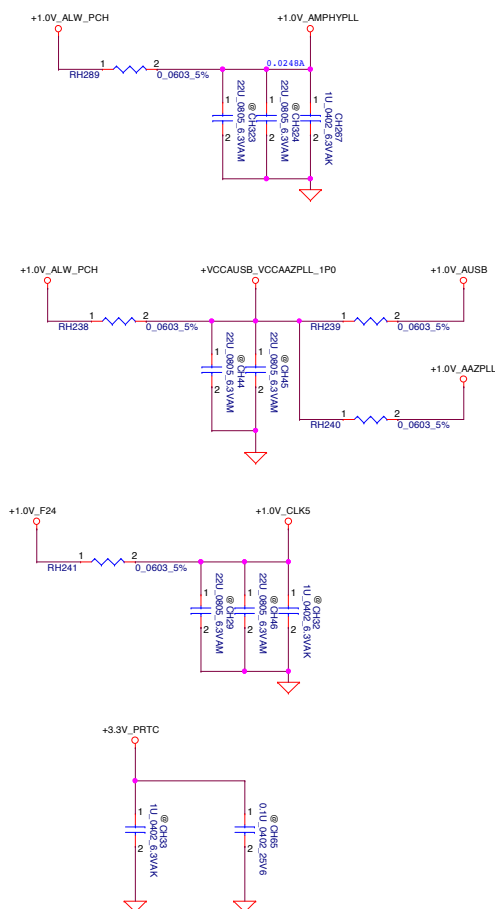




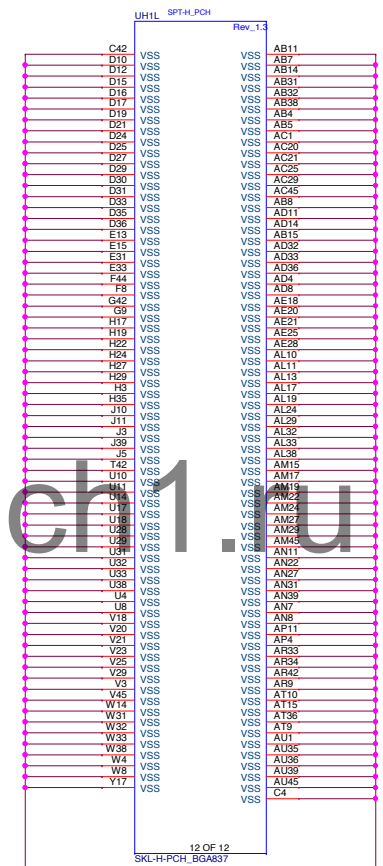
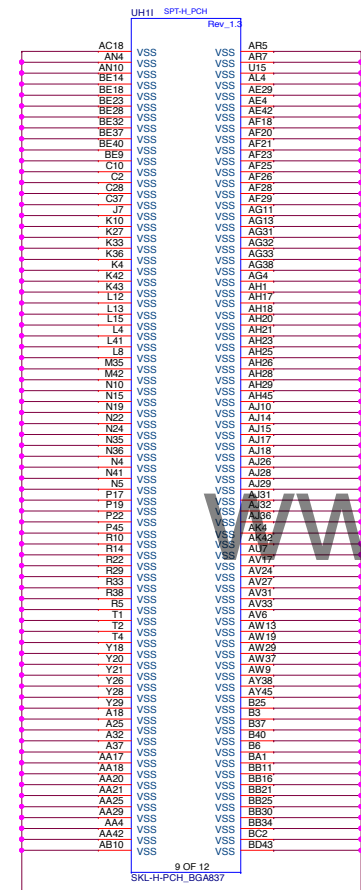
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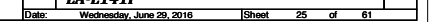
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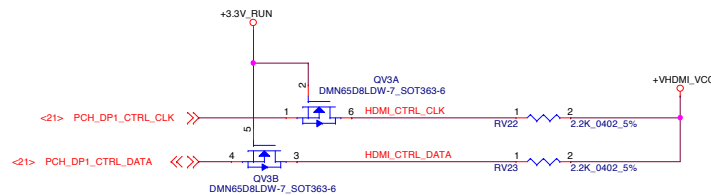
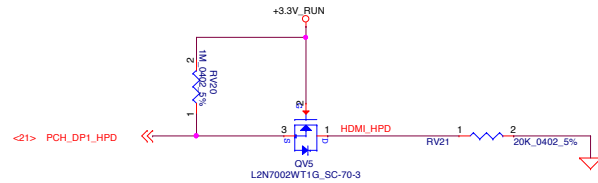
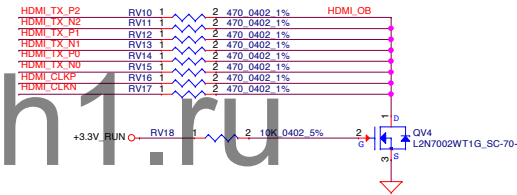
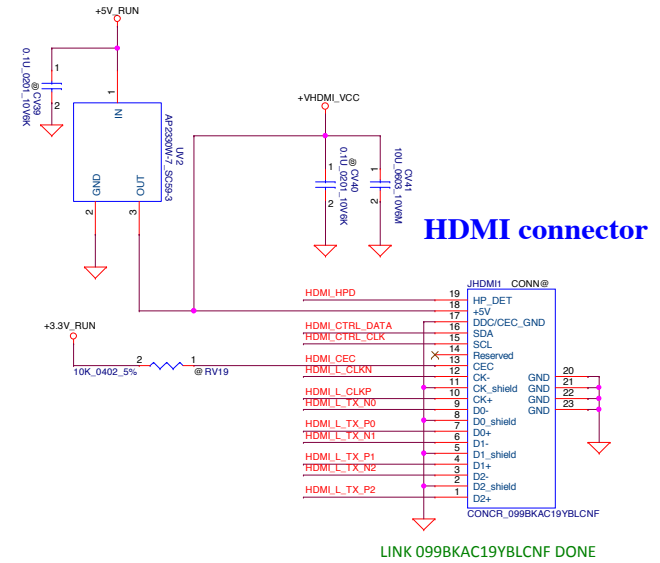
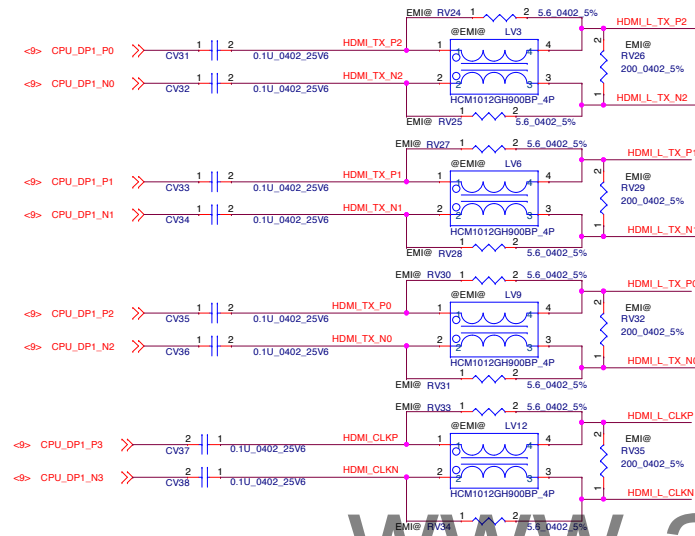


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				Date: Wednesday, June 29, 2016		Sheet	23 of 61





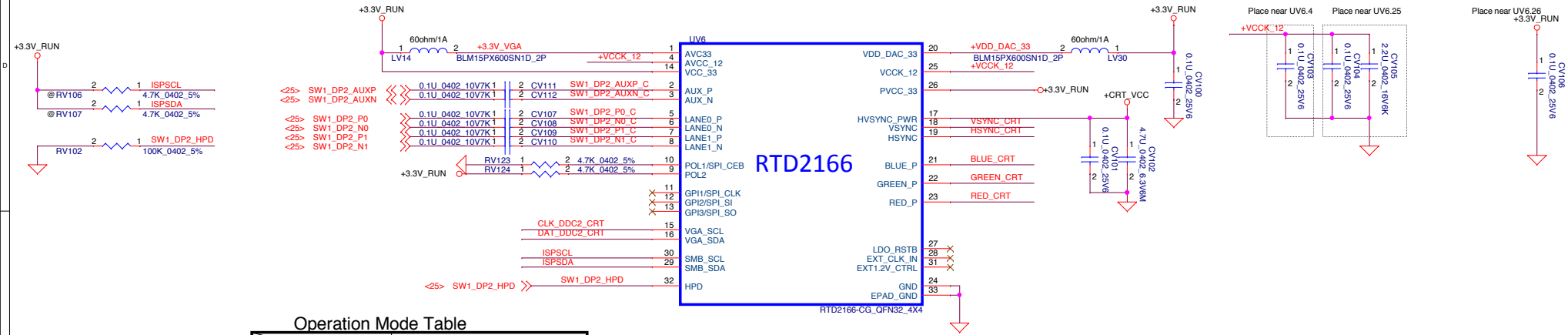
For Breckenridge 14



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61											

For TBT SW2_DP2
For non-TBT SW1_DP2

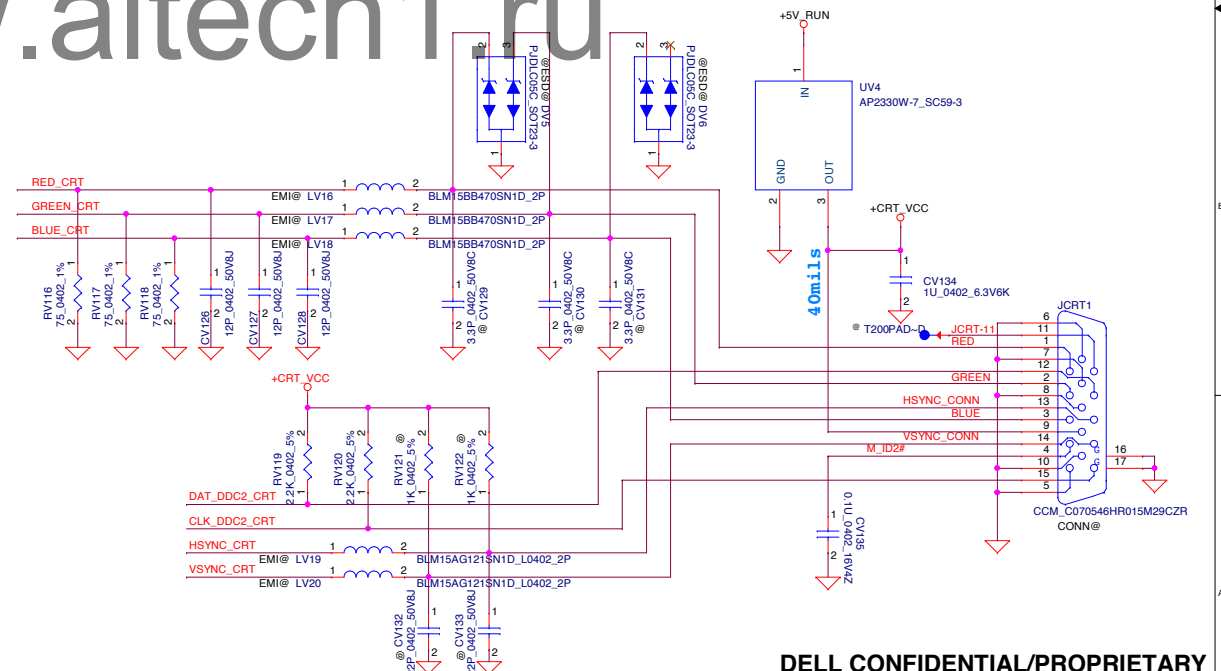
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM

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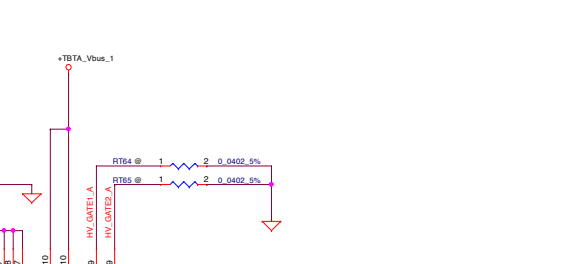
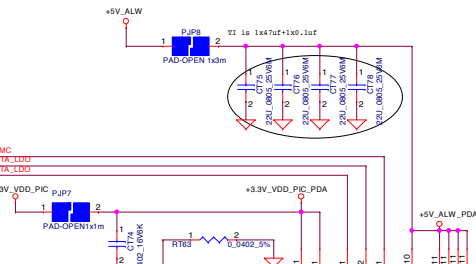
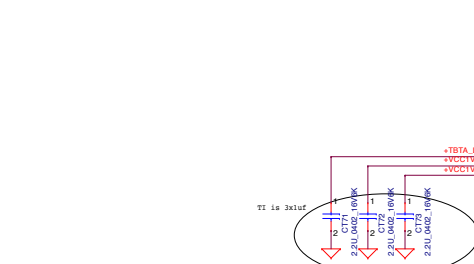
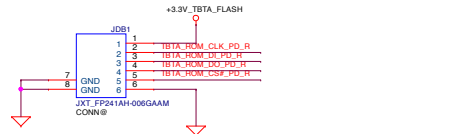
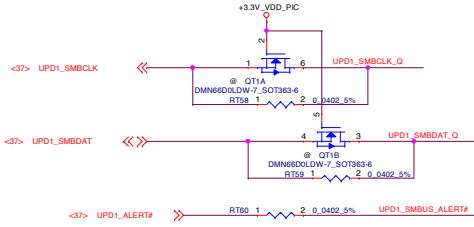
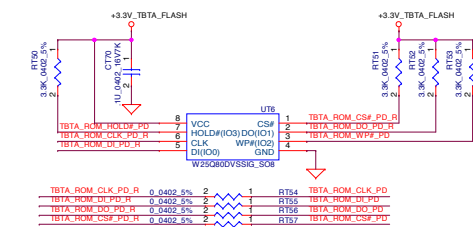
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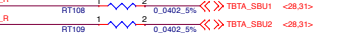
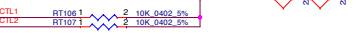
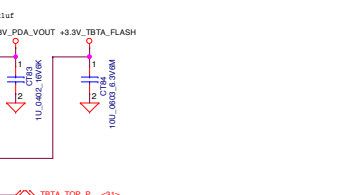
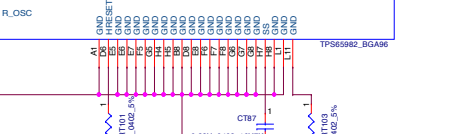
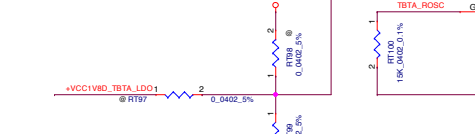
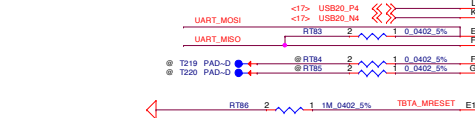
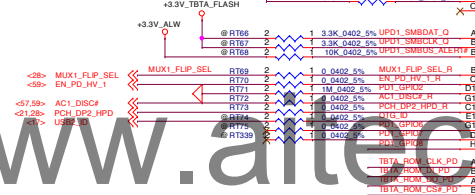
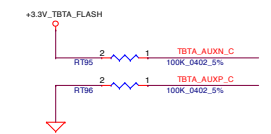
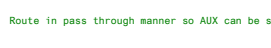
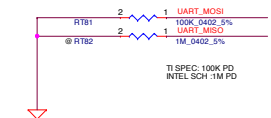
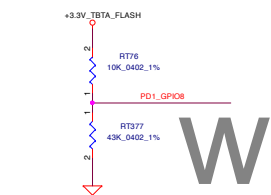
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For Non-AR config



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	<p>UEP only</p> <p>SV @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>Ti VID supported</p>
0.10	0.18	1	<p>UEP only</p> <p>SV @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configuration Ti VID supported</p>
0.20	0.28	2	<p>UEP only</p> <p>SV @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>Ti VID supported</p>
0.30	0.38	3	<p>UEP only</p> <p>SV @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configuration Ti VID supported</p>
0.40	0.48	4	<p>DPP</p> <p>SV @0.9-3.0A Sink capability</p> <p>SV @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>Ti VID supported</p> <p>Accepts data and power role swaps, but does not initiate.</p>
0.50	0.58	5	<p>DPP</p> <p>SV @0.9-3.0A Sink capability</p> <p>SV @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>Ti VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swap to UEP- and can initiate.</p>
0.60	0.68	6	<p>DPP</p> <p>SV @0.9-3.0A Sink capability</p> <p>SV @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>Ti VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swap to UEP- and can initiate.</p>
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.



Need Link TPS65982D

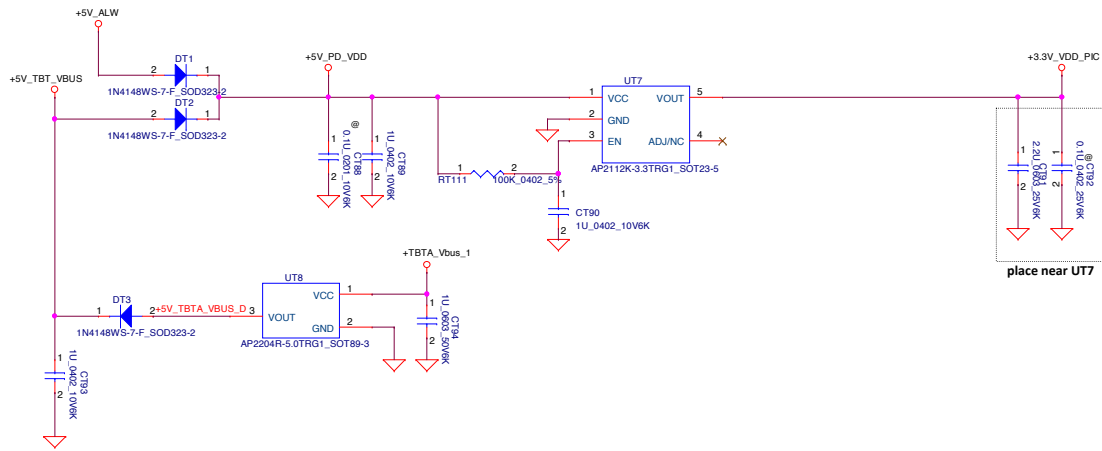
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				Type Number	[Type] C/PD Controller TI
				Date	LA-E141P
				Wednesday, June 29, 2016	Sheet 29 of 61

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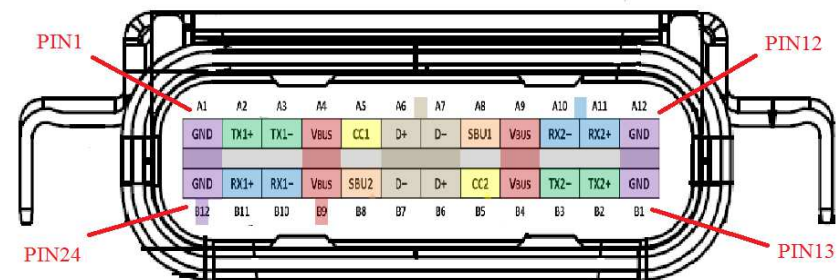
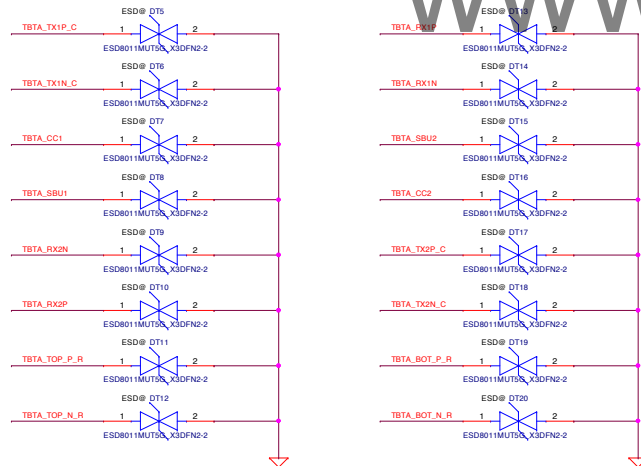
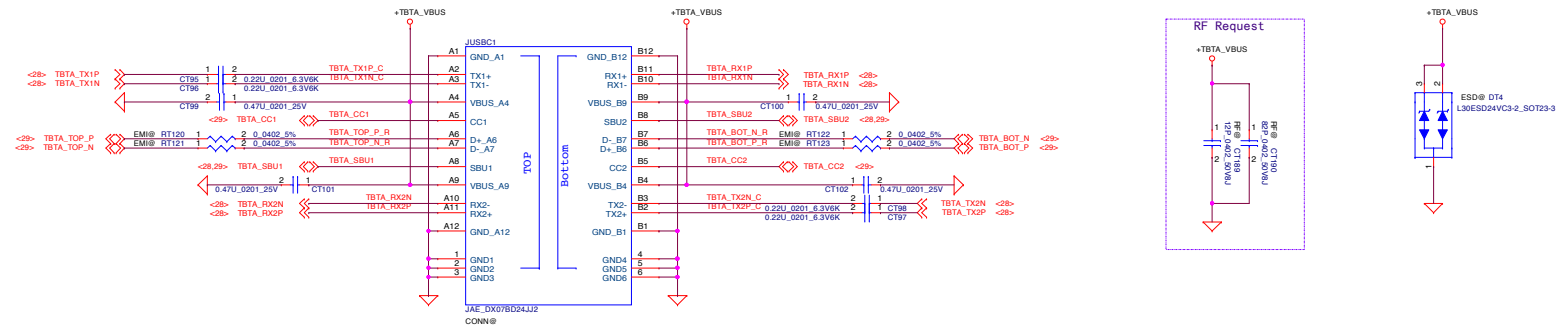
[Type C]PD Controller TH

Size C	Document Number	Rev
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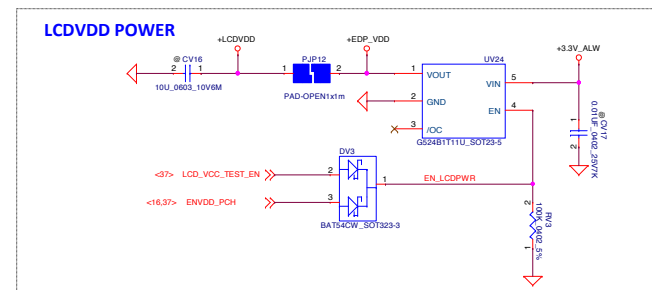
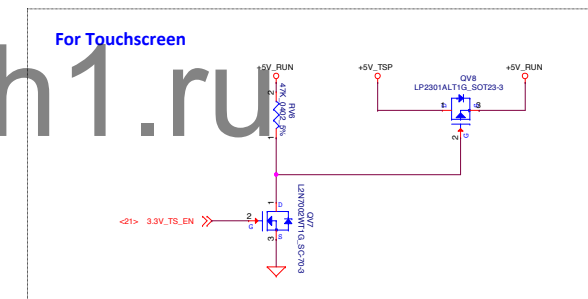
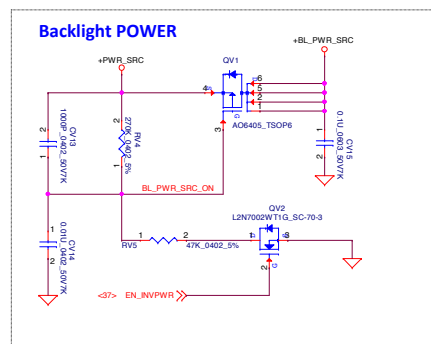
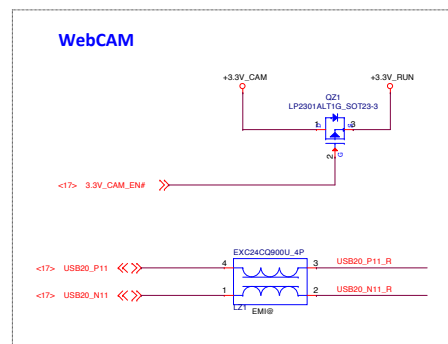
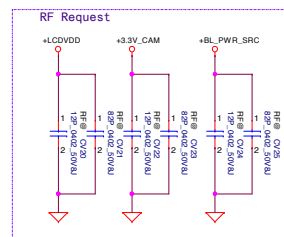
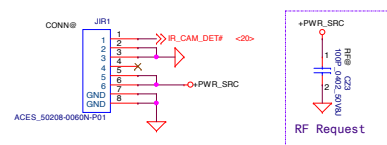
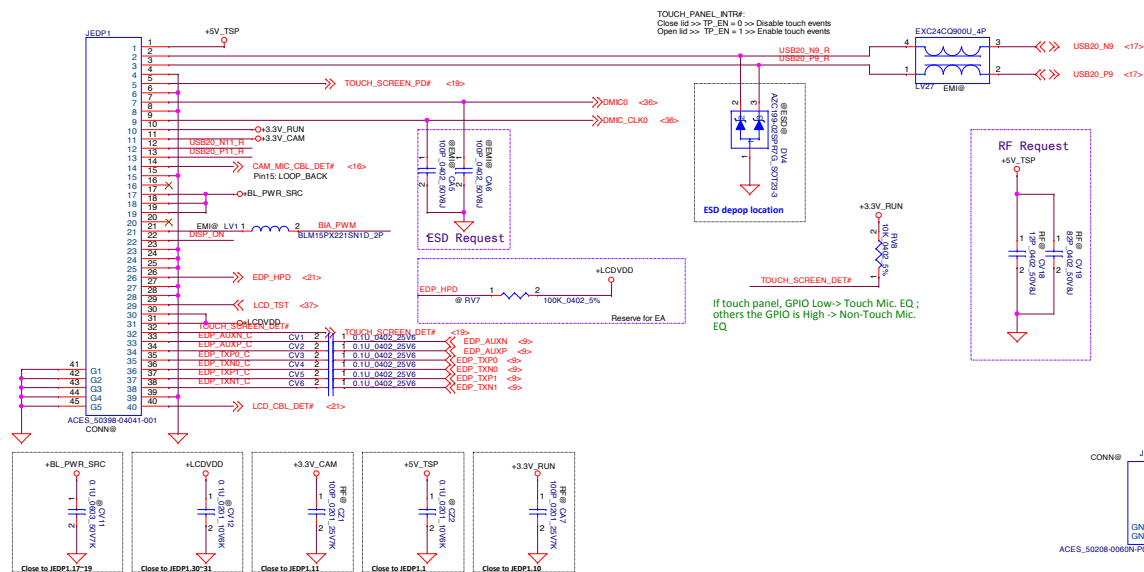


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LA-E141P		0.2		Date: Wednesday, June 29, 2016	
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For Breckenridge 14

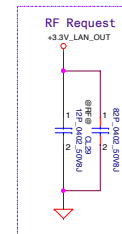
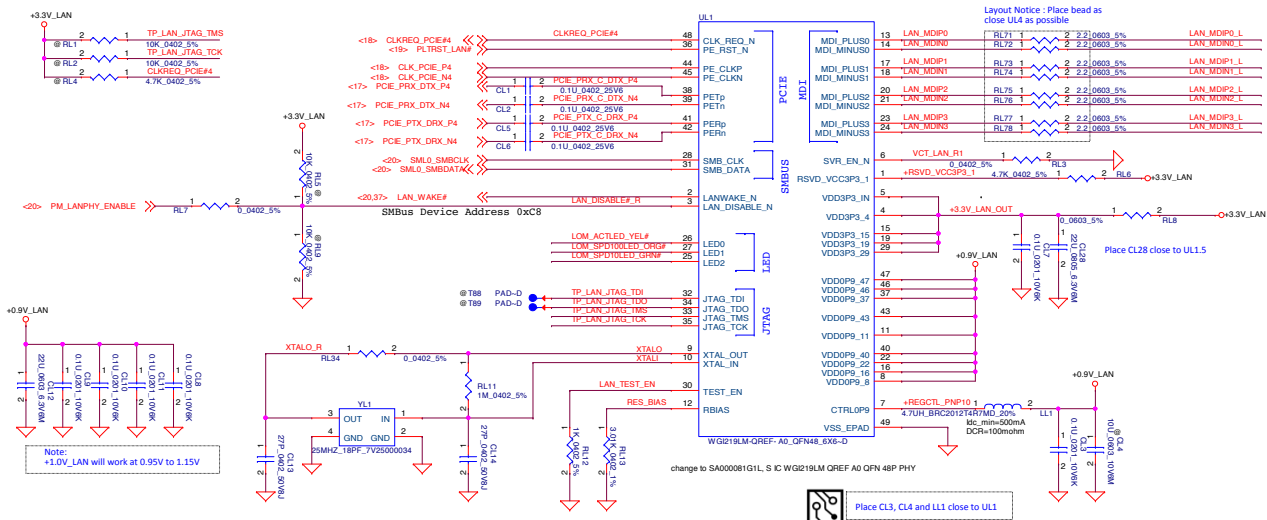


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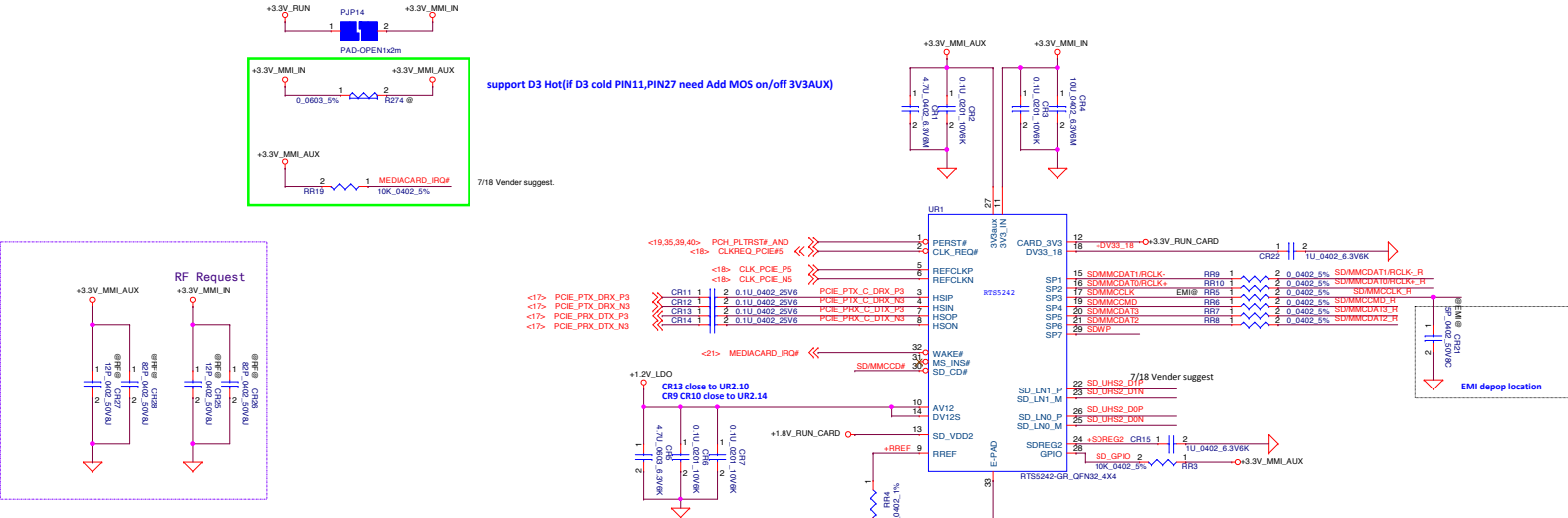
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eDP CONN & Touch screen

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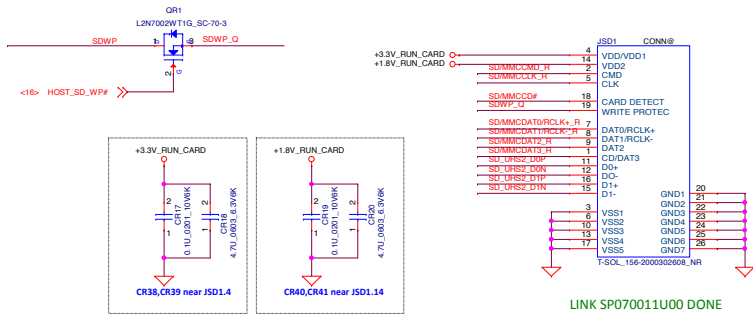


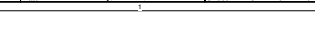
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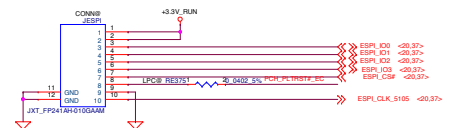
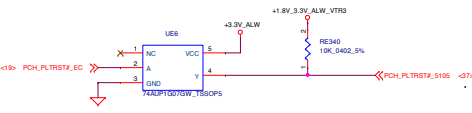


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HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
High	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
Low	Low	High	Write Protect(FW LOCK)

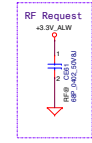
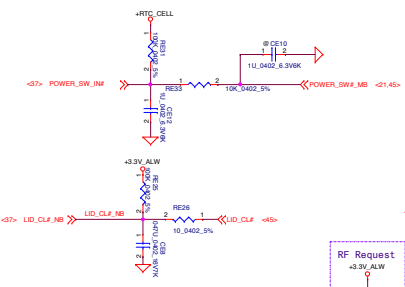




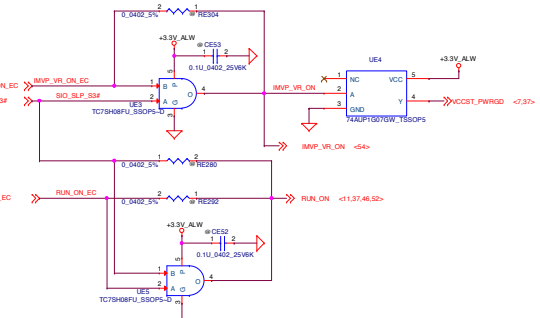
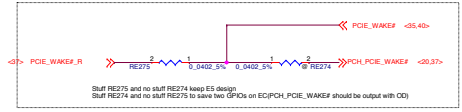


LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

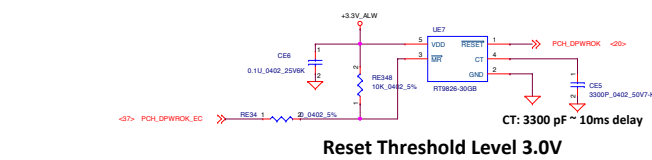


RE79	CE40	REV
240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	BR15 H
4.3K	4700p	BR15 P

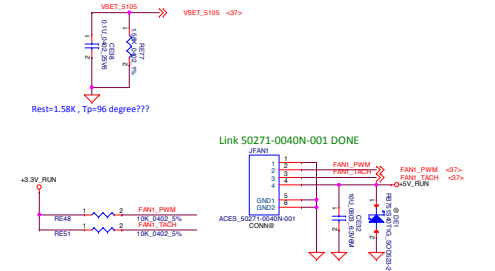
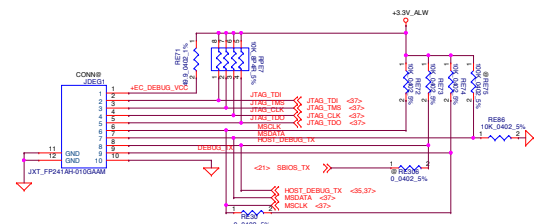
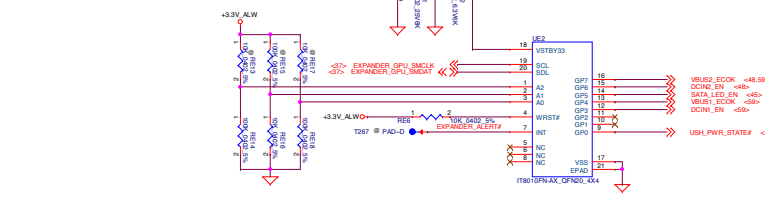
PP: ACE_DETH rise time is measured from 5%~68% BOARD_ID rise time is measured from 5%~68% PANEL_ID rise time is measured from 5%~68%

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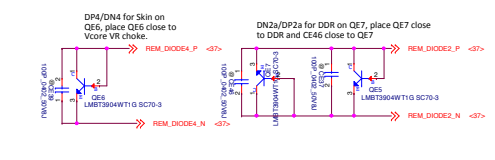
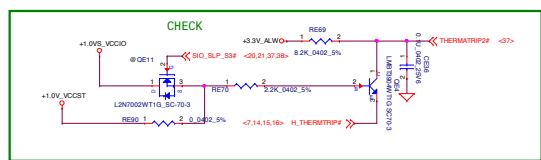
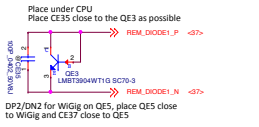


Control Byte
0 1 0 0 A2 A1 A0 R/W
R/W = 0 = Write
R/W = 1 = Read

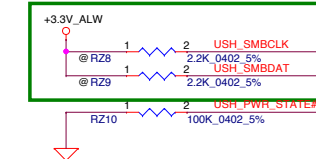
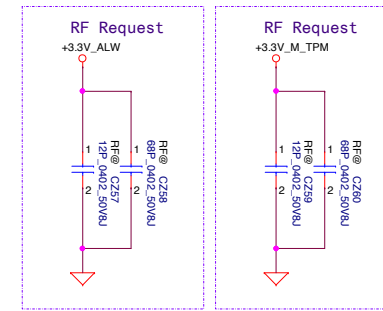
SMbus address 0x40



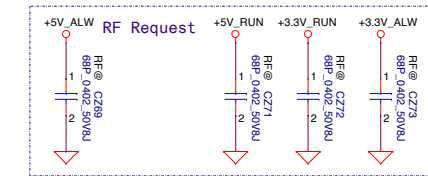
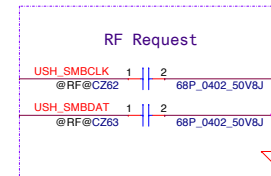
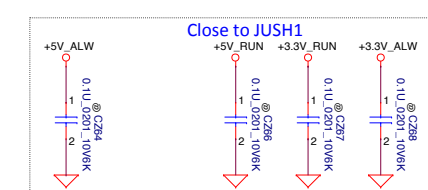
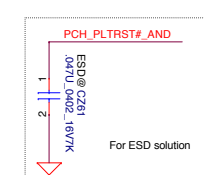
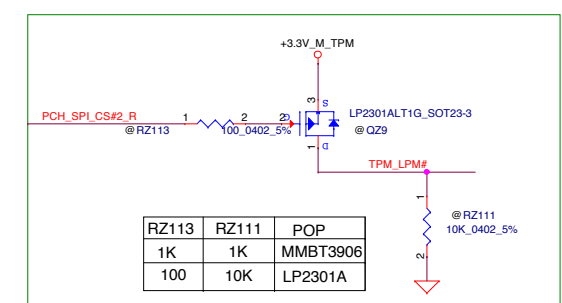
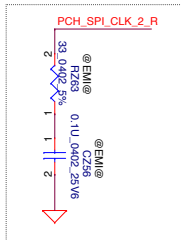
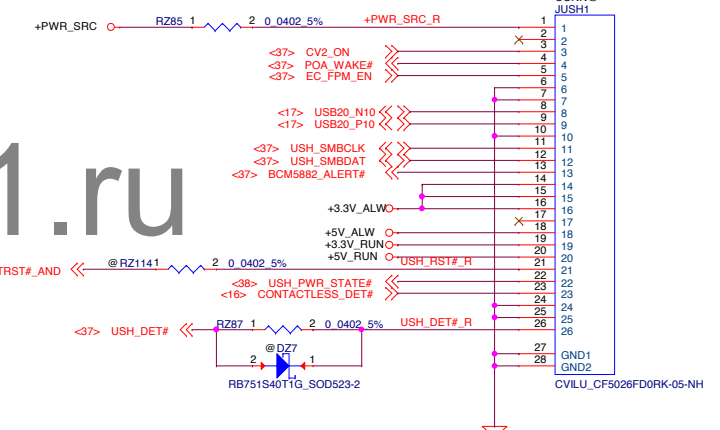
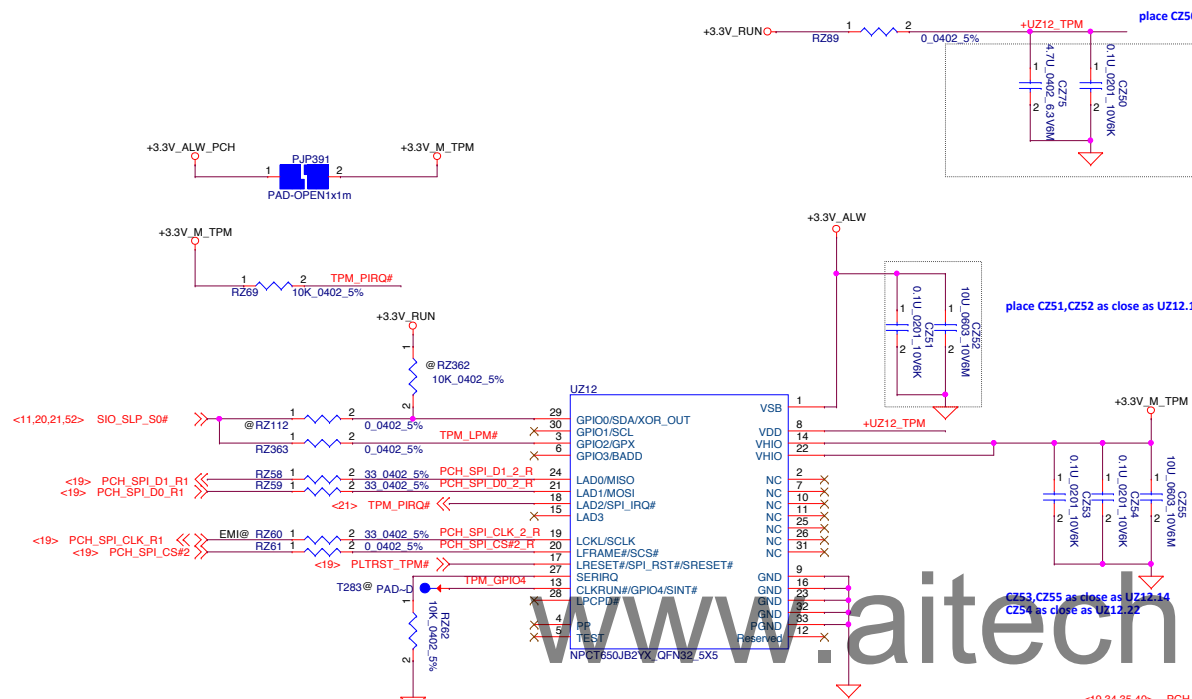
5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



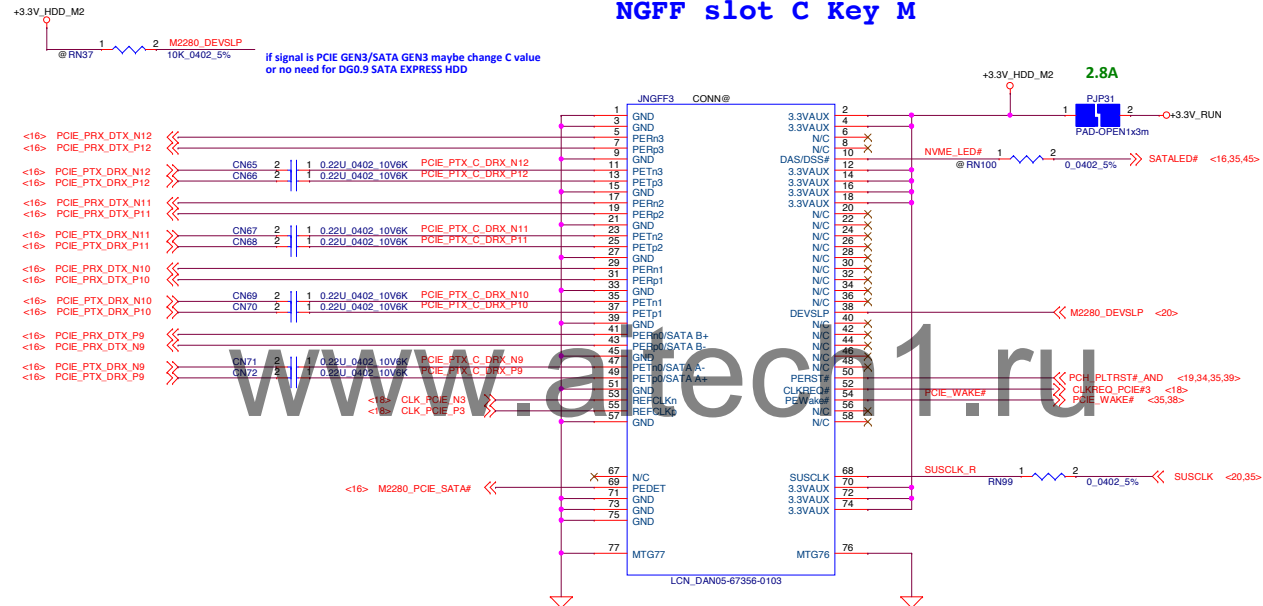
For NUVOTON TPM



USH CONN



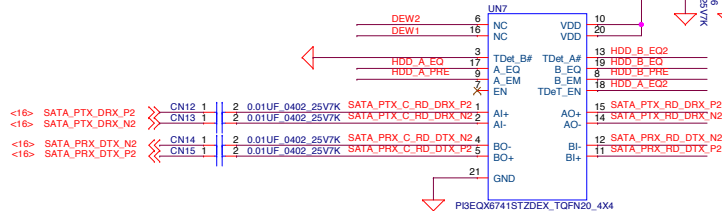
NGFF slot C Key M



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				Date	Wednesday, June 29, 2016
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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDeT_B#	NC	TDeT_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

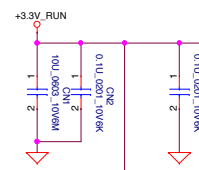
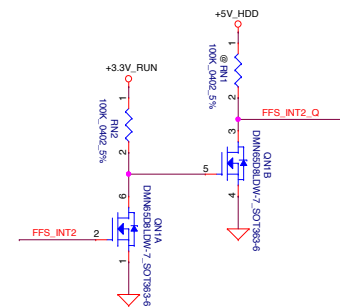
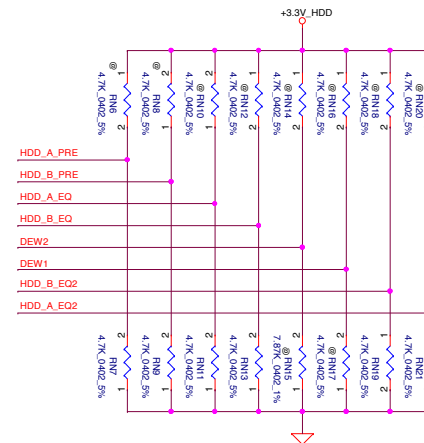
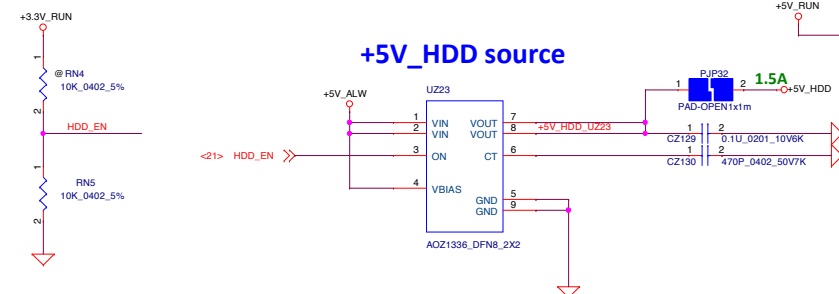
SATA Repeater



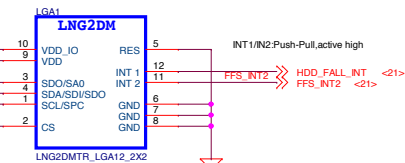
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	PD (RN5)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 9dB 14dB	7dB 9dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 NC 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB

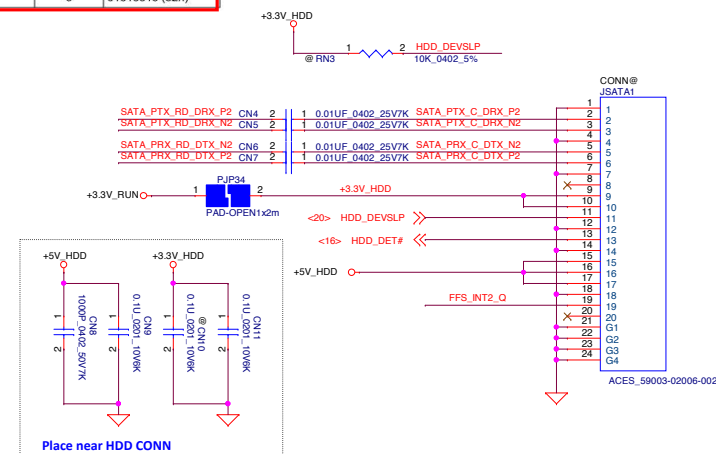
* red color is current setting



Free Fall Sensor



Command	SAD[6:1]	SAD[0] = S_A0	R/W	SAD+R/W
Read	010100	0	0	01010001 (51h)
Write	010100	0	1	01010000 (50h)
Read	010100	1	0	01010011 (53h)
Write	010100	1	1	01010010 (52h)

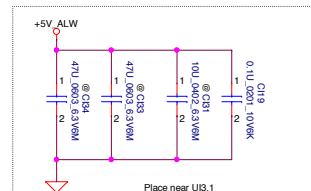
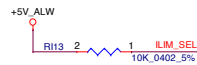
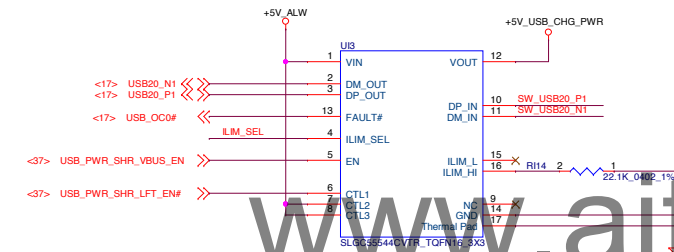
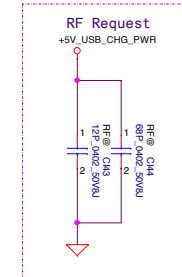
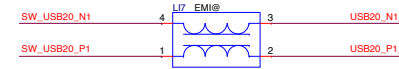
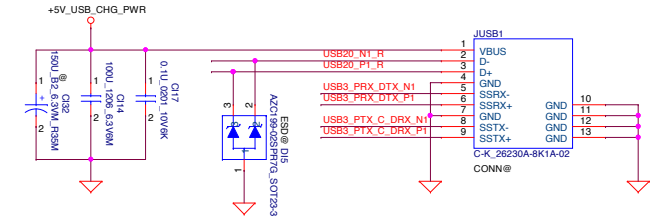
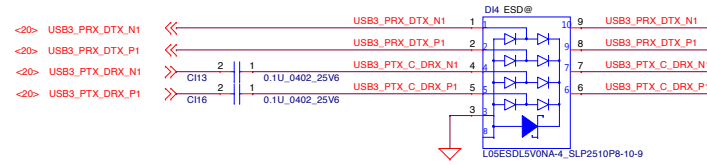


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Title	HDD CONN		
Size	Document Number	Rev	0.2
B	LA-E141P		
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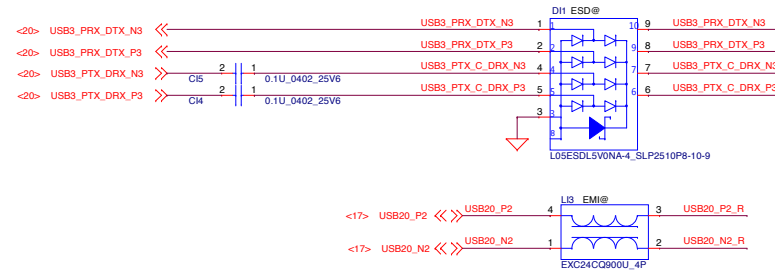
For PWR SW + Charger combine IC



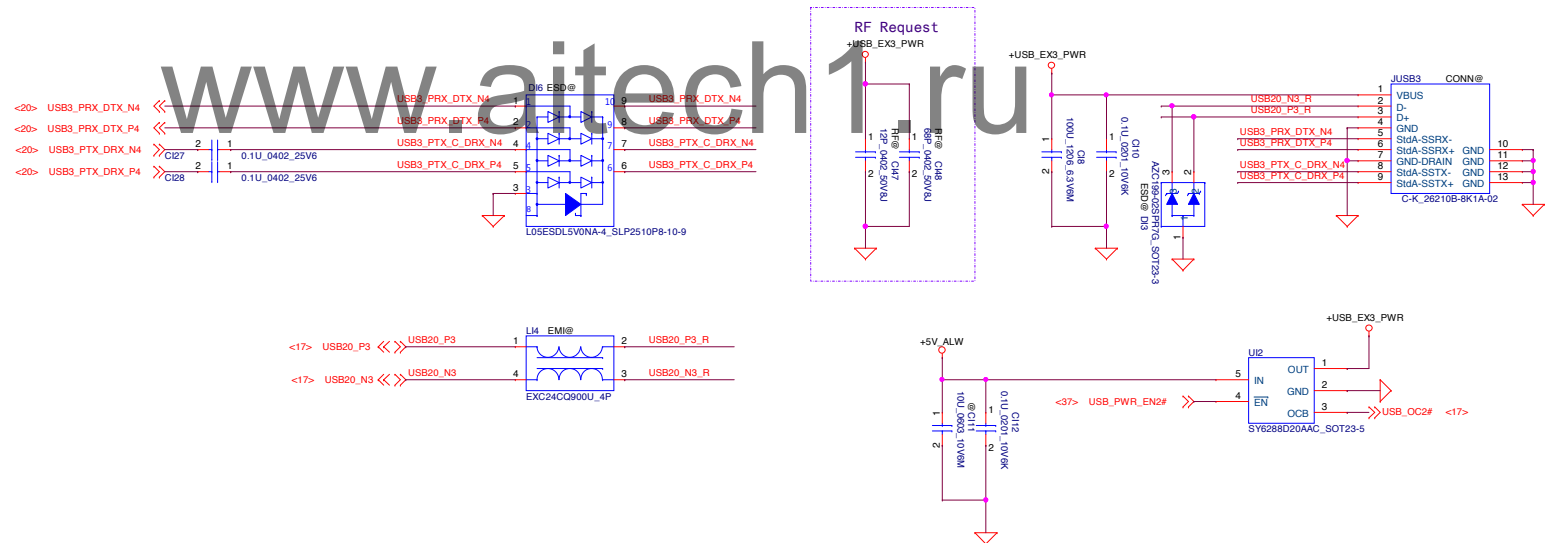
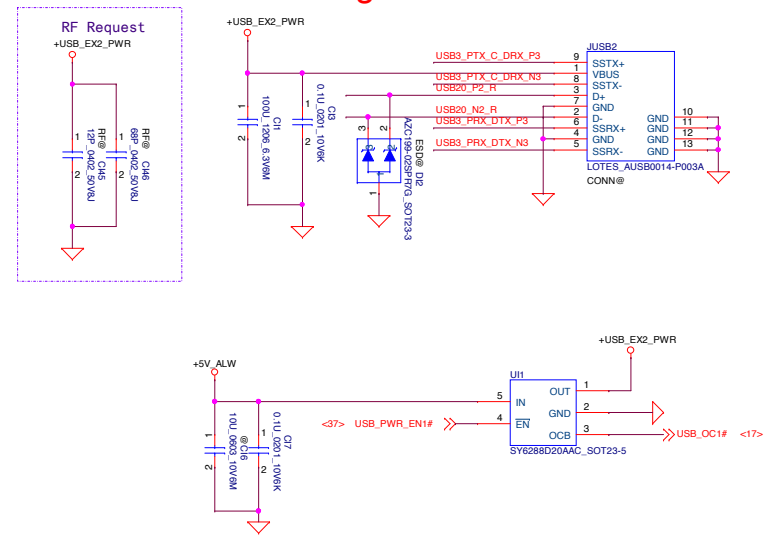
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For Breckenridge 14&15/Steamboat 14

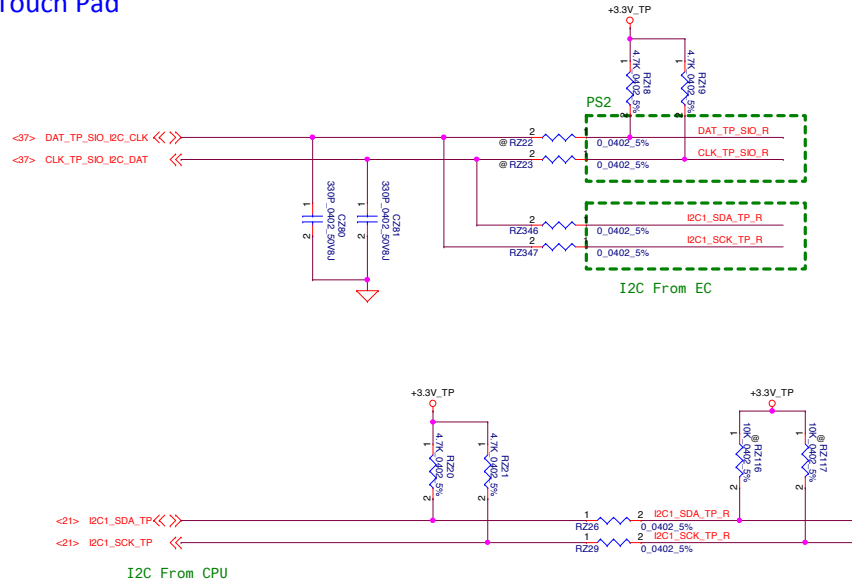


DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

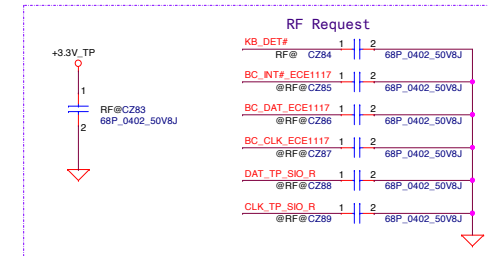
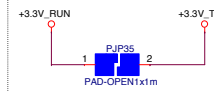


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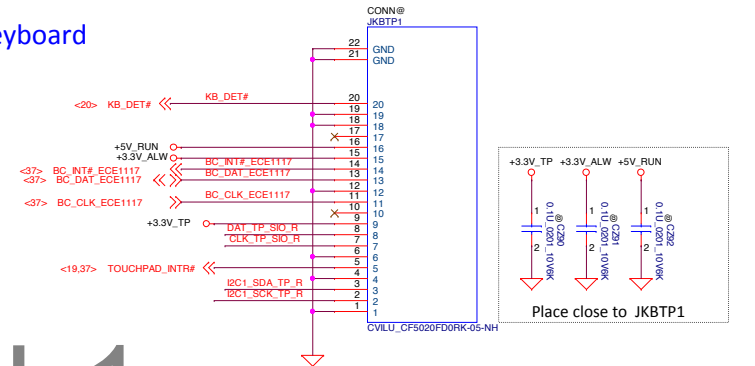
Touch Pad



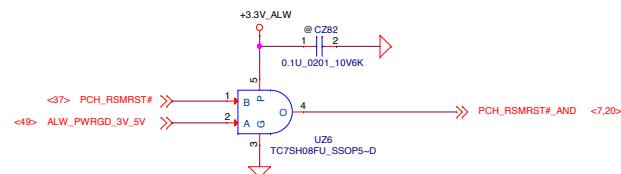
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7). For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows. Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



Keyboard

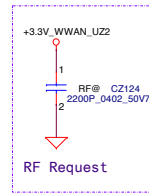
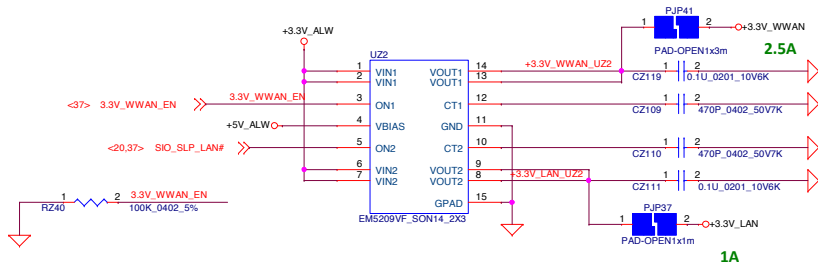


RSMRST circuit

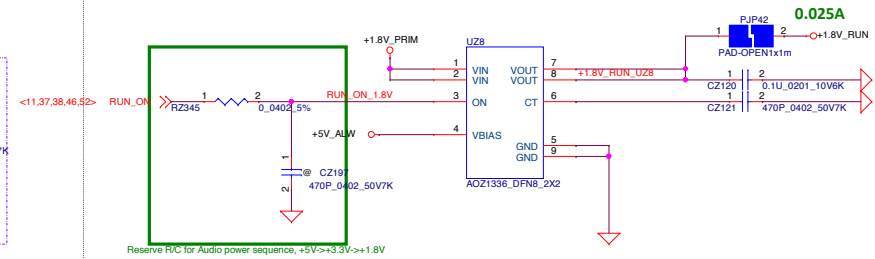


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							Keyboard
							Document Number
							LA-E141P
							Rev
							0.2
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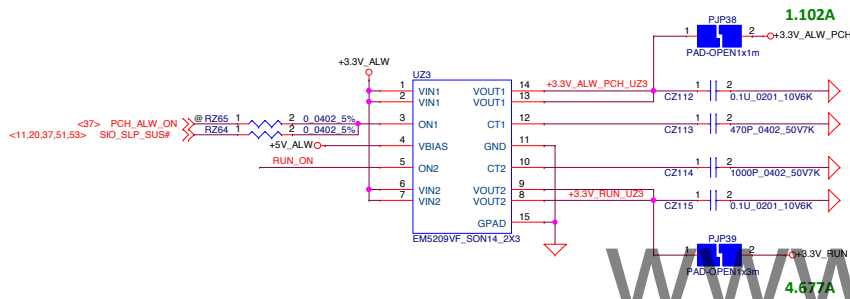
+3.3V_WWAN/+3.3V_LAN source



+1.8V_RUN source

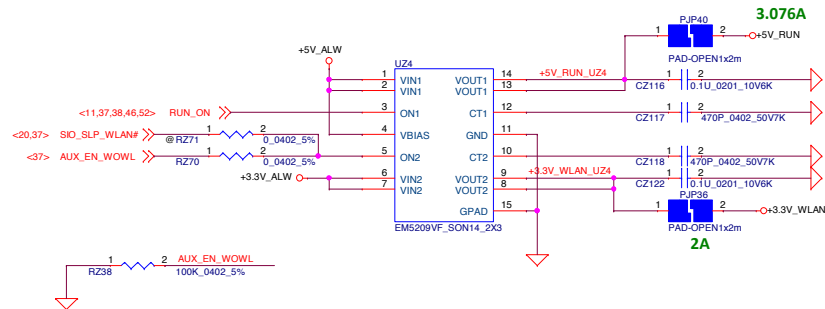


+3.3V_ALW_PCH/+3.3V_RUN source



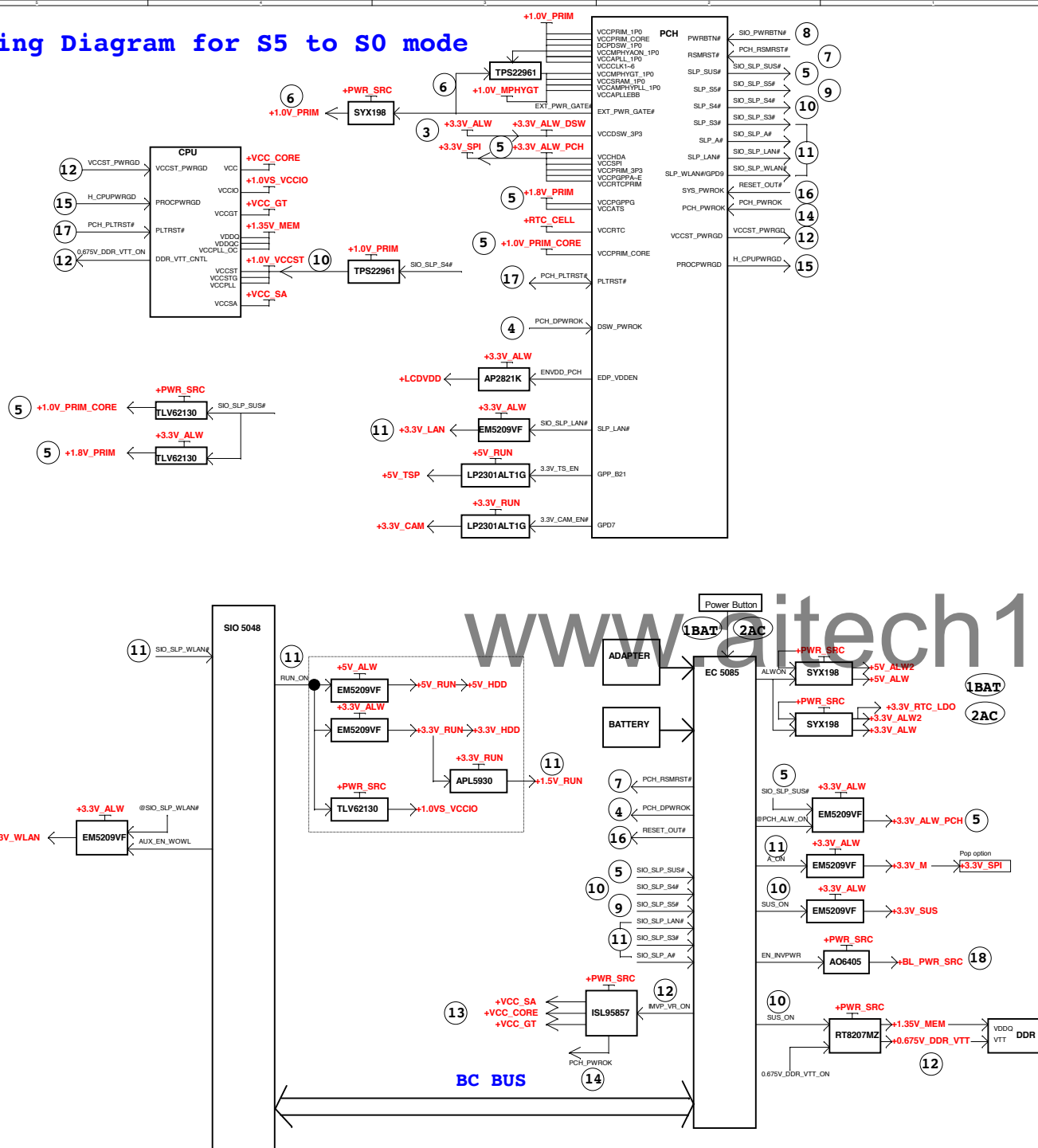
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+5V_RUN/+3.3V_WLAN source

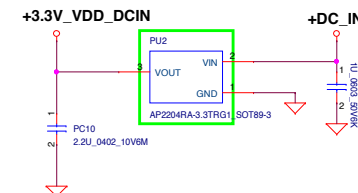
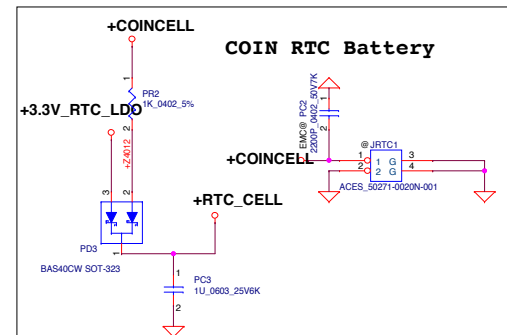
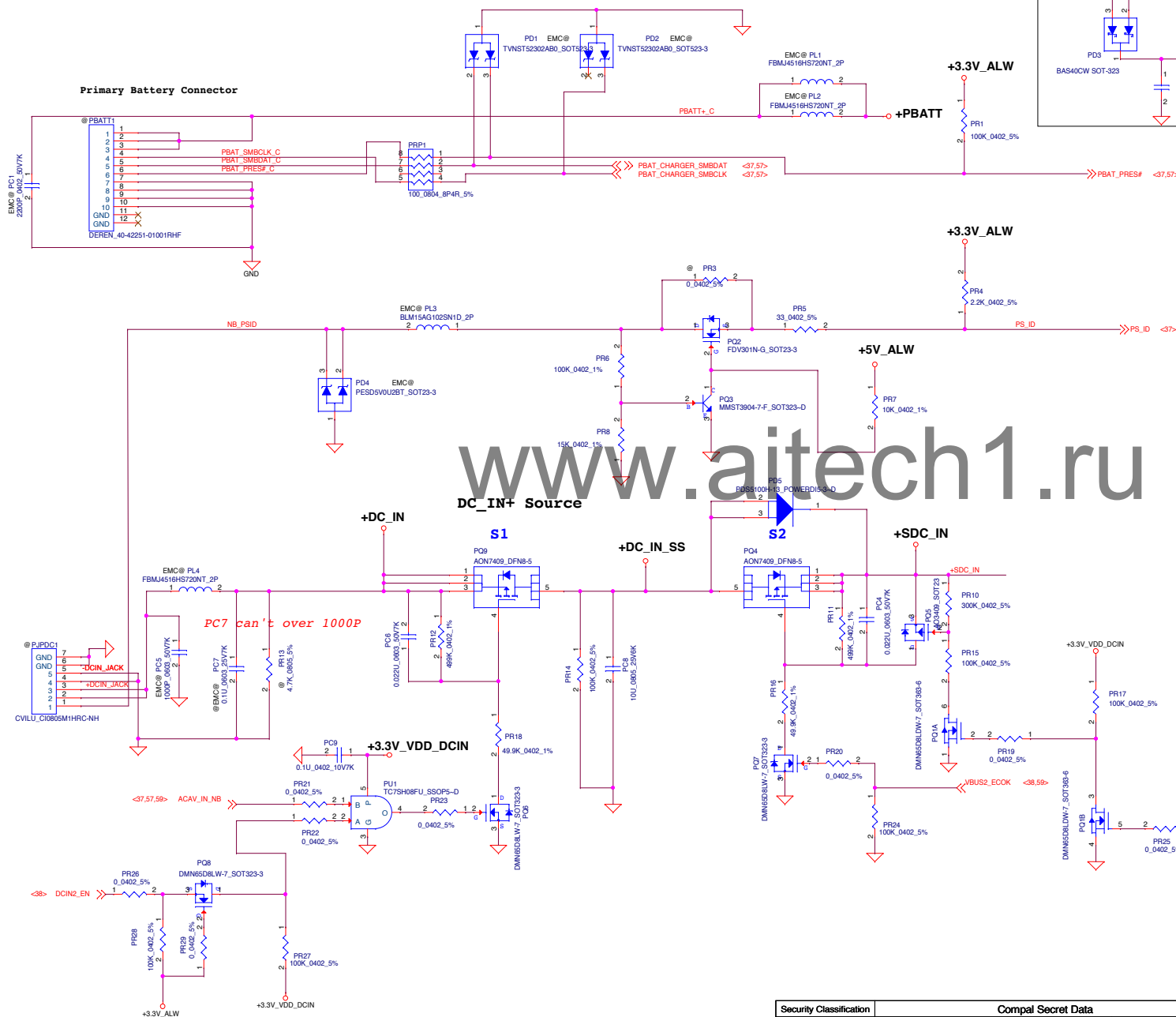


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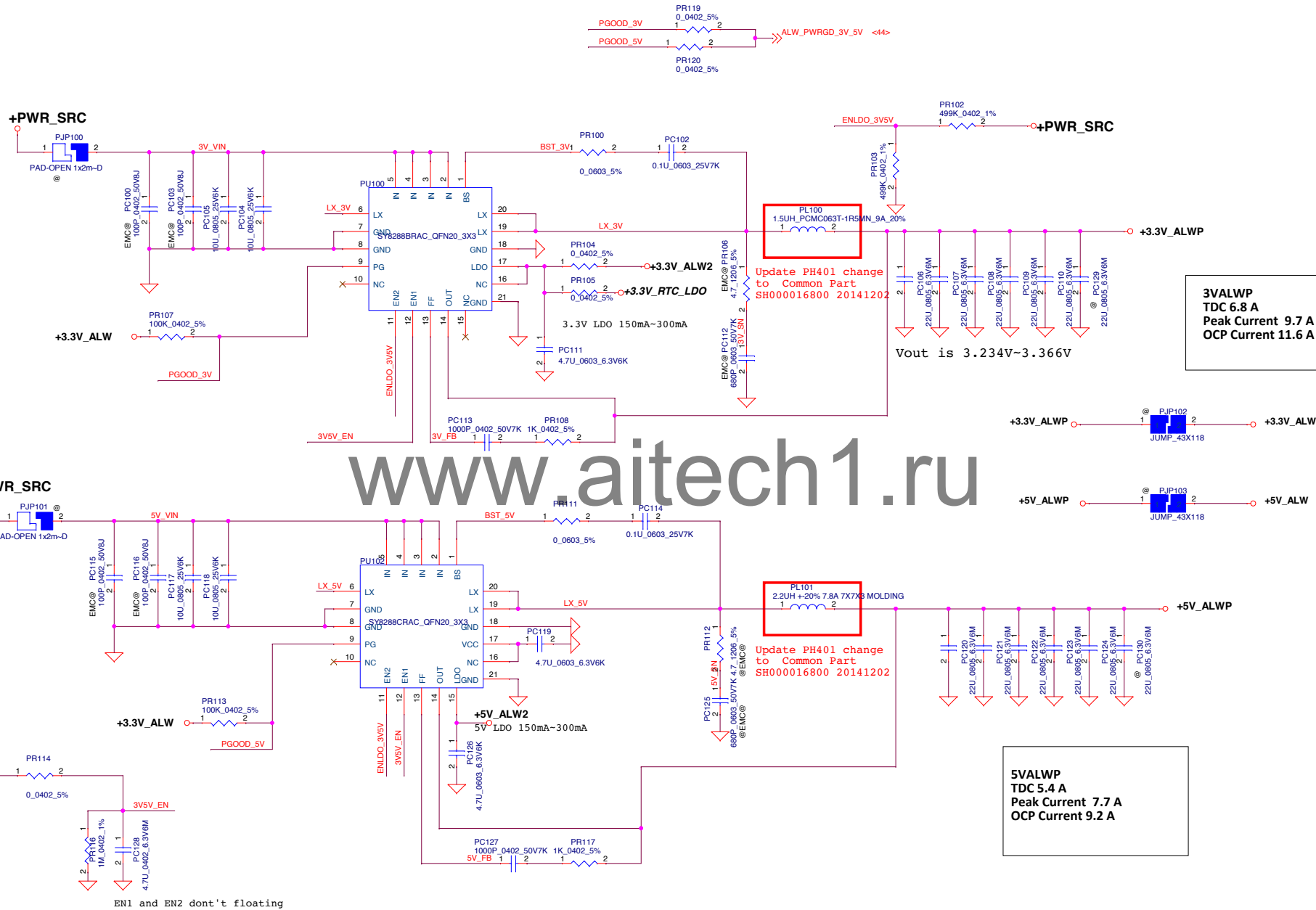
Timing Diagram for S5 to S0 mode



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			Date Wednesday, May 30, 2001	
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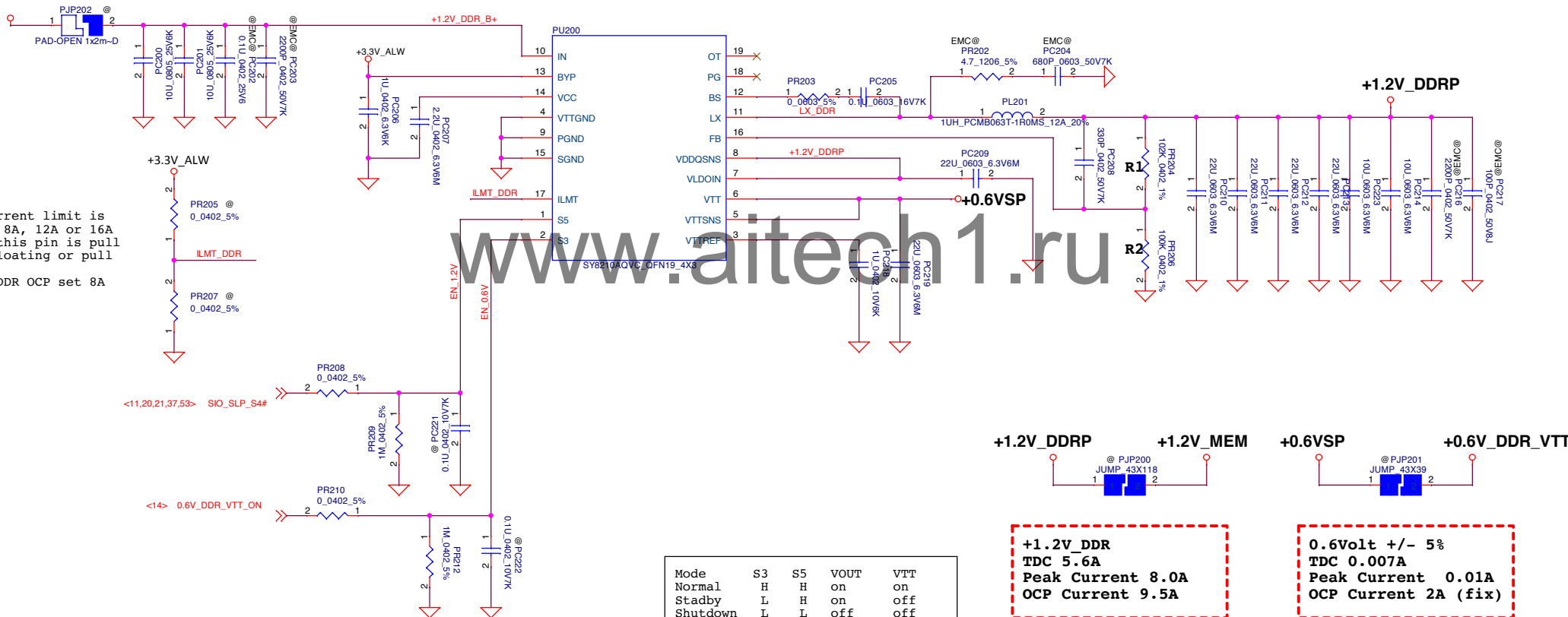


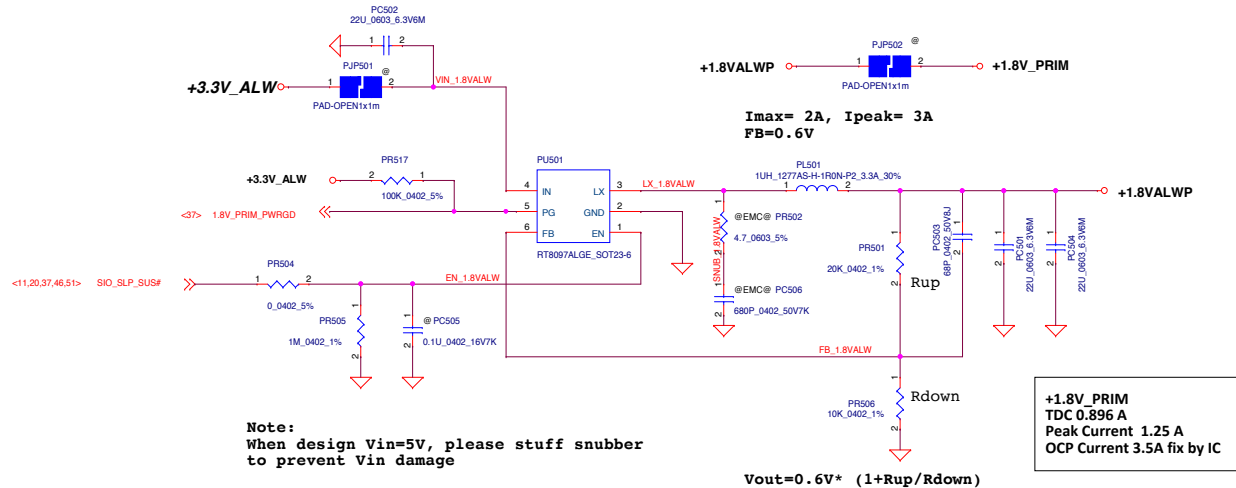
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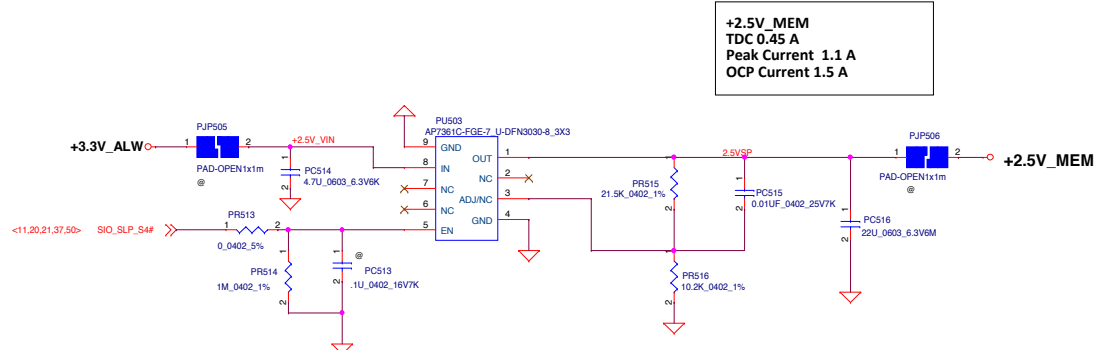
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+PWR_SRC

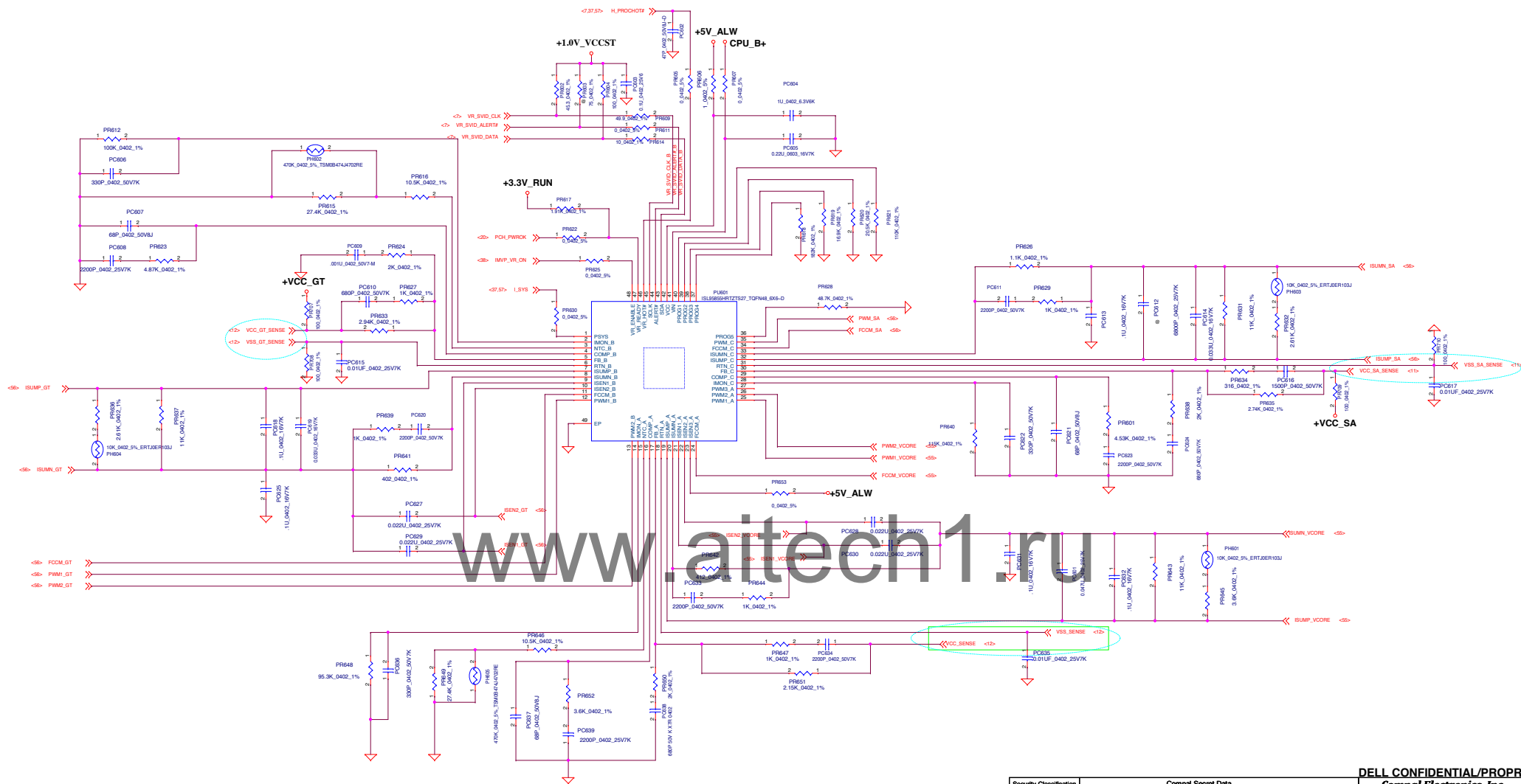




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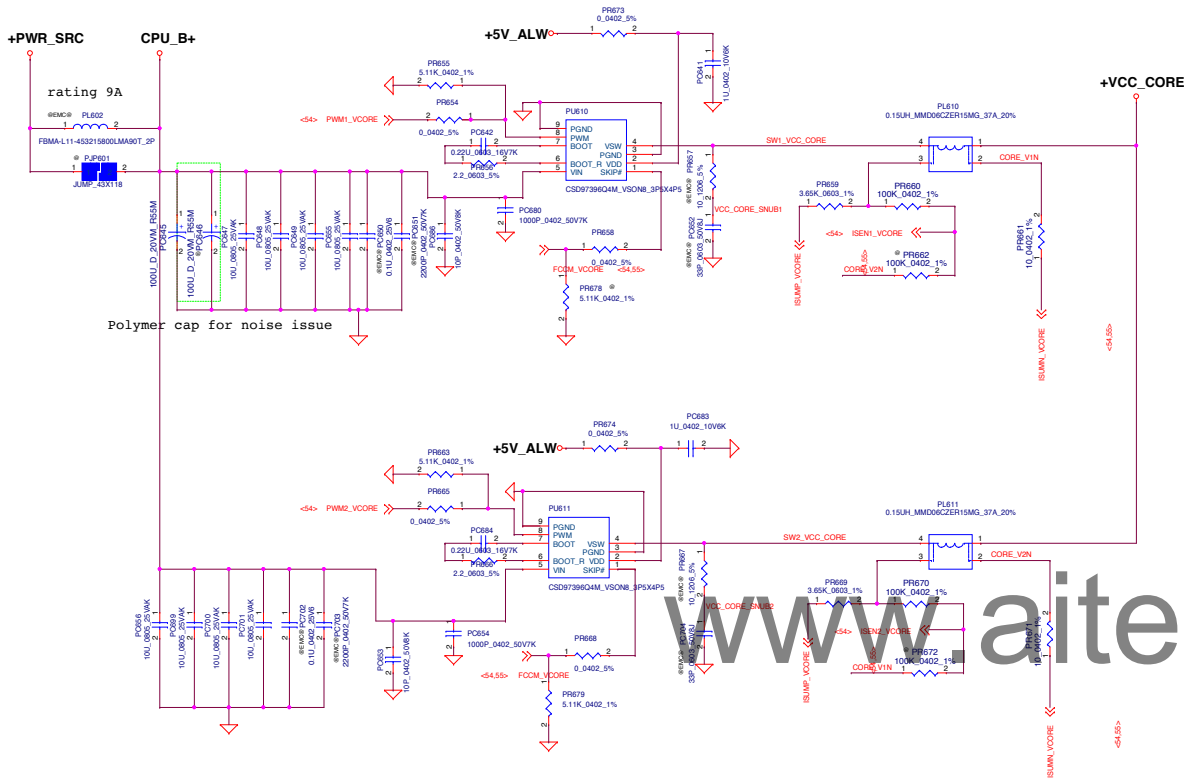


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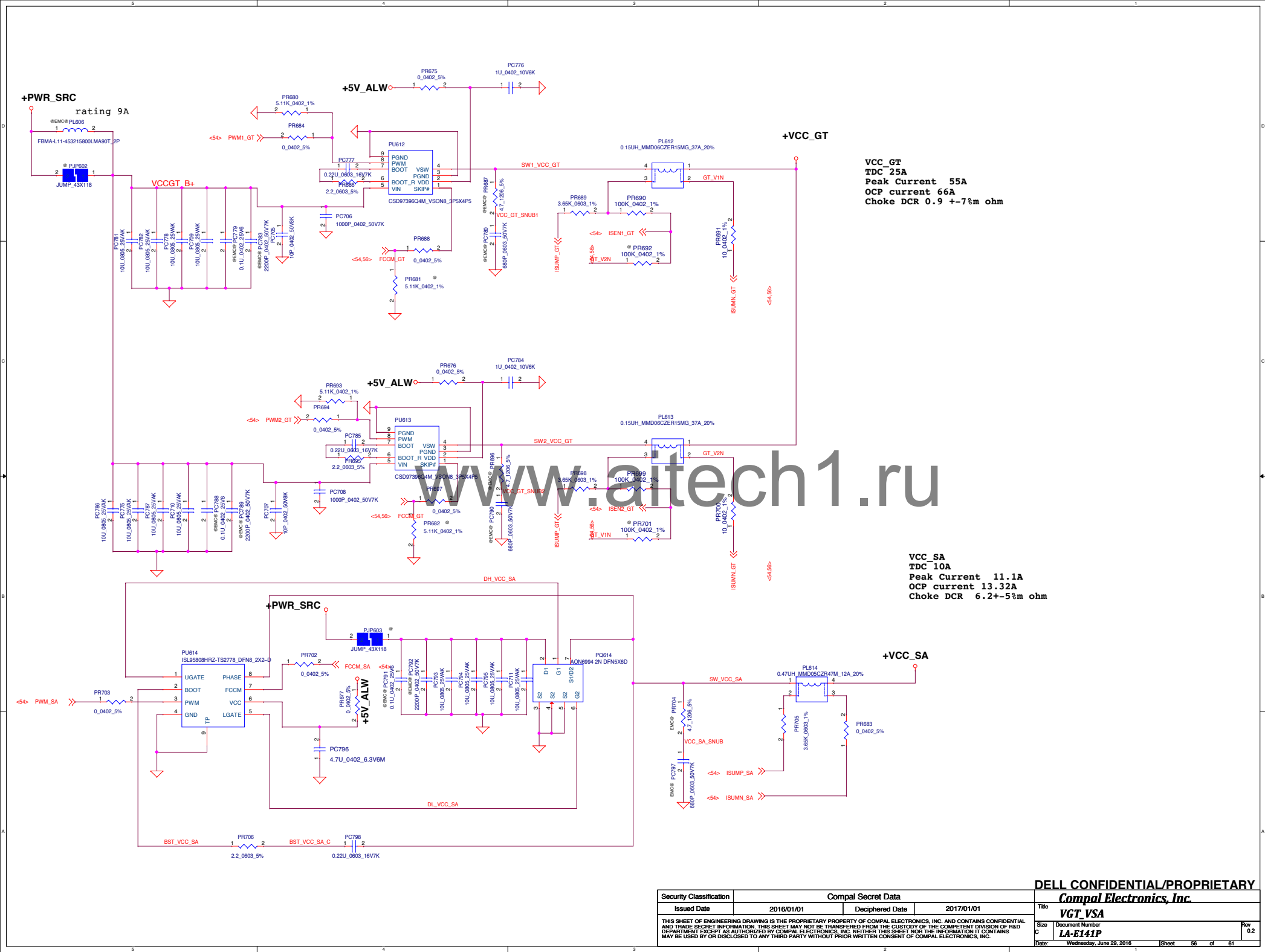
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Title		VCORE ISL95855	
Revision		1.0	
Date		Wednesday, June 29, 2016	

VCC_core
TDC 50A
Peak Current 60A
OCP current 81.6A
Choke DCR 0.9 +-7% ohm



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Title				DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc.			
VCCORE							
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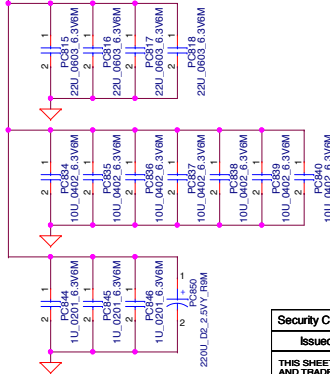
VCC_CORE Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side.
22U_0603 * 8 pcs+330u_D2*2 pcs

+VCC_CORE



VCC_SA Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs

+VCC_SA



VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs +470u_D2*2 pcs

+VCC_GT



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

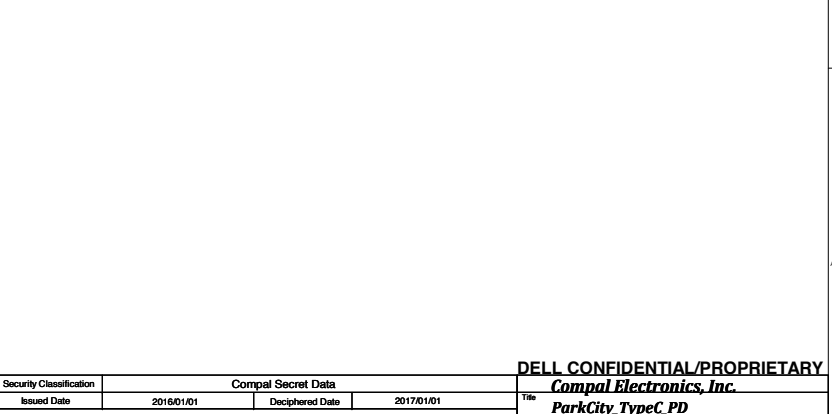
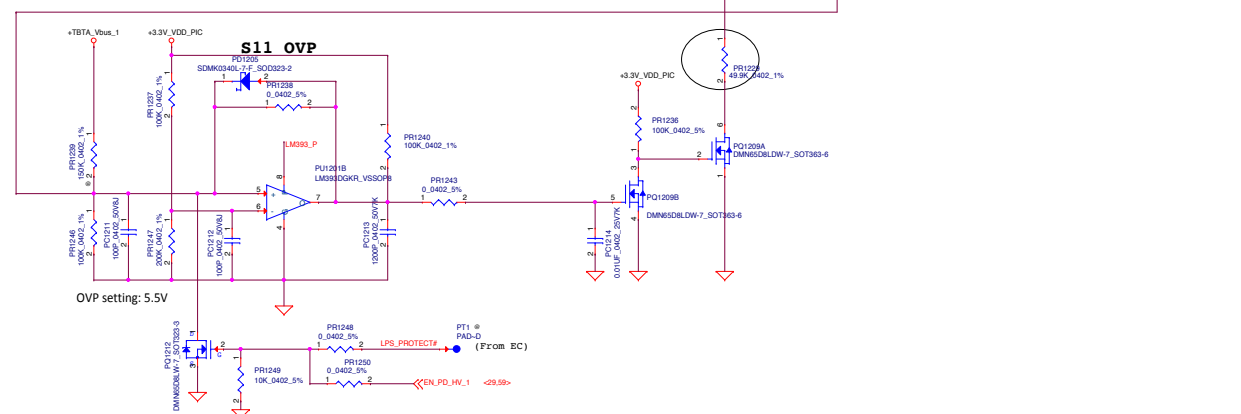
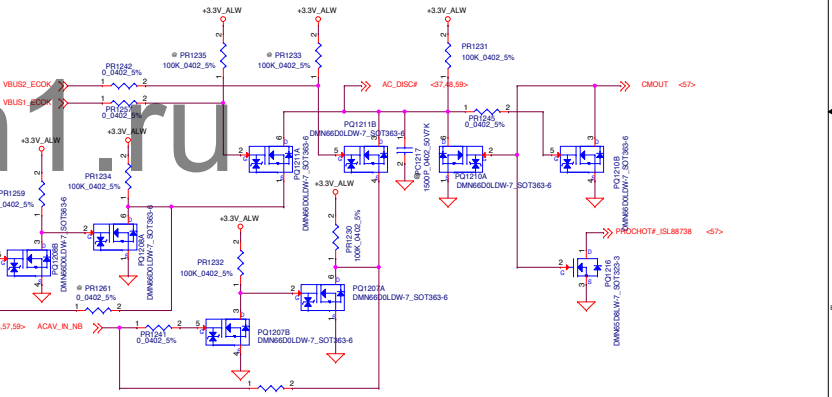
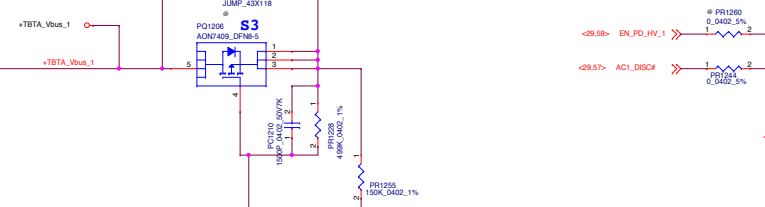
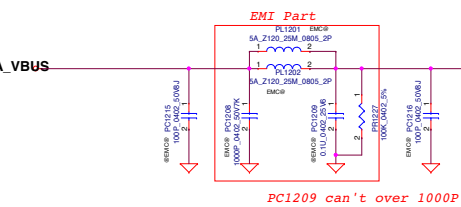
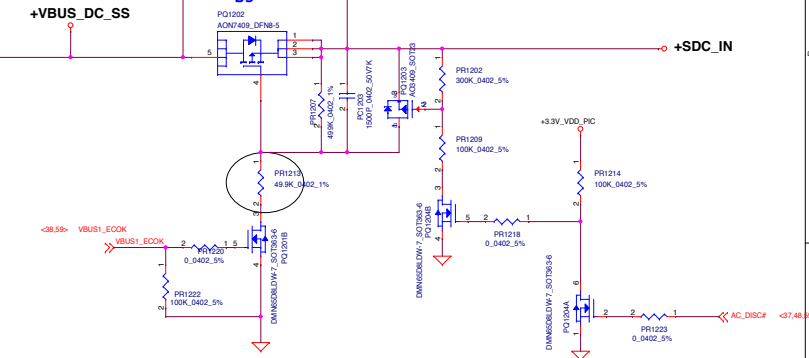
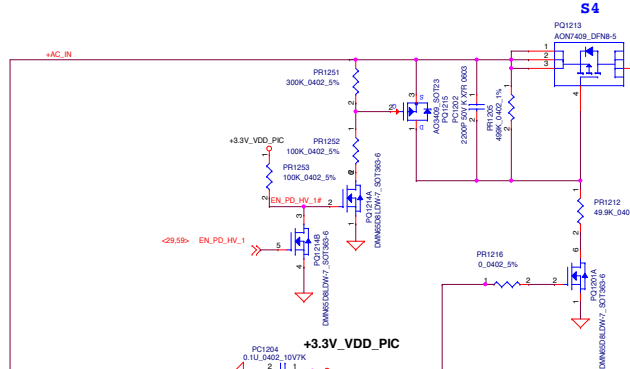
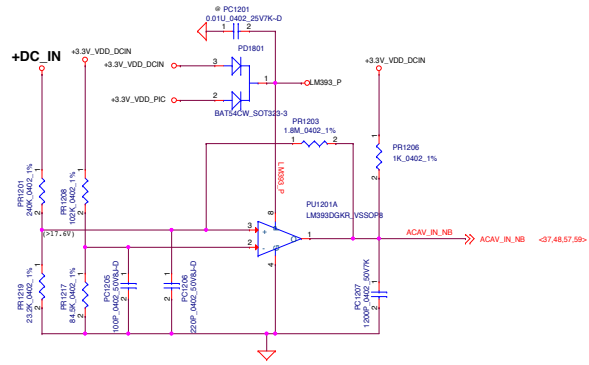
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Compal Electronics, Inc.
PROCESSOR DECOUPLING

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DCIN_AC_Detector



Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	2016/5/27	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
2	37	HW	2016/5/27	COMPAL	Reserve PORT80_DET# PD resistance	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
3	35	HW	2016/6/1	COMPAL	Intel schematics reivew modify item	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(0.0201 to 10uF_0603	0.2(X01)
4	39	HW	2016/6/1	COMPAL	TPM change to NUVOTON	Change TPM from Atmel to NUVOTON.	0.2(X01)
5	35	HW	2016/6/1	COMPAL	Intel reviwie result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
6	35	HW	2016/6/7	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
7	37	HW	2016/6/7	COMPAL	For MEC5105K-D1-TN setting	1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361	0.2(X01)
8	35,32	HW	2016/6/16	COMPAL	For EMC request	De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00	0.2(X01)
9	41	HW	2016/6/16	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	POP RN5	0.2(X01)
10	39	ME	2016/6/17	COMPAL	Connector change	1. JKBTP1 change to CVILU CF5020FD0RK-05-NH 2. JUSH1 change to CVILU CF5026FD0RK-05-NH 3. JIR1 change to ACES_50208-0060N-P01	0.2(X01)
11	36	HW	2016/6/20	COMPAL	Vender suggest	RA7,RA8 change to 16.2ohm	0.2(X01)
12	37	HW	2016/6/22	COMPAL	The possibility of GPIO map update	Add RE514,RE515 for RTCRST_ON	0.2(X01)
13	41	HW	2016/6/22	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)

Security Classification		Compal Secret Data		TITLE Compal Electronics, Inc.	
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